



Arm® Morello System Development Platform

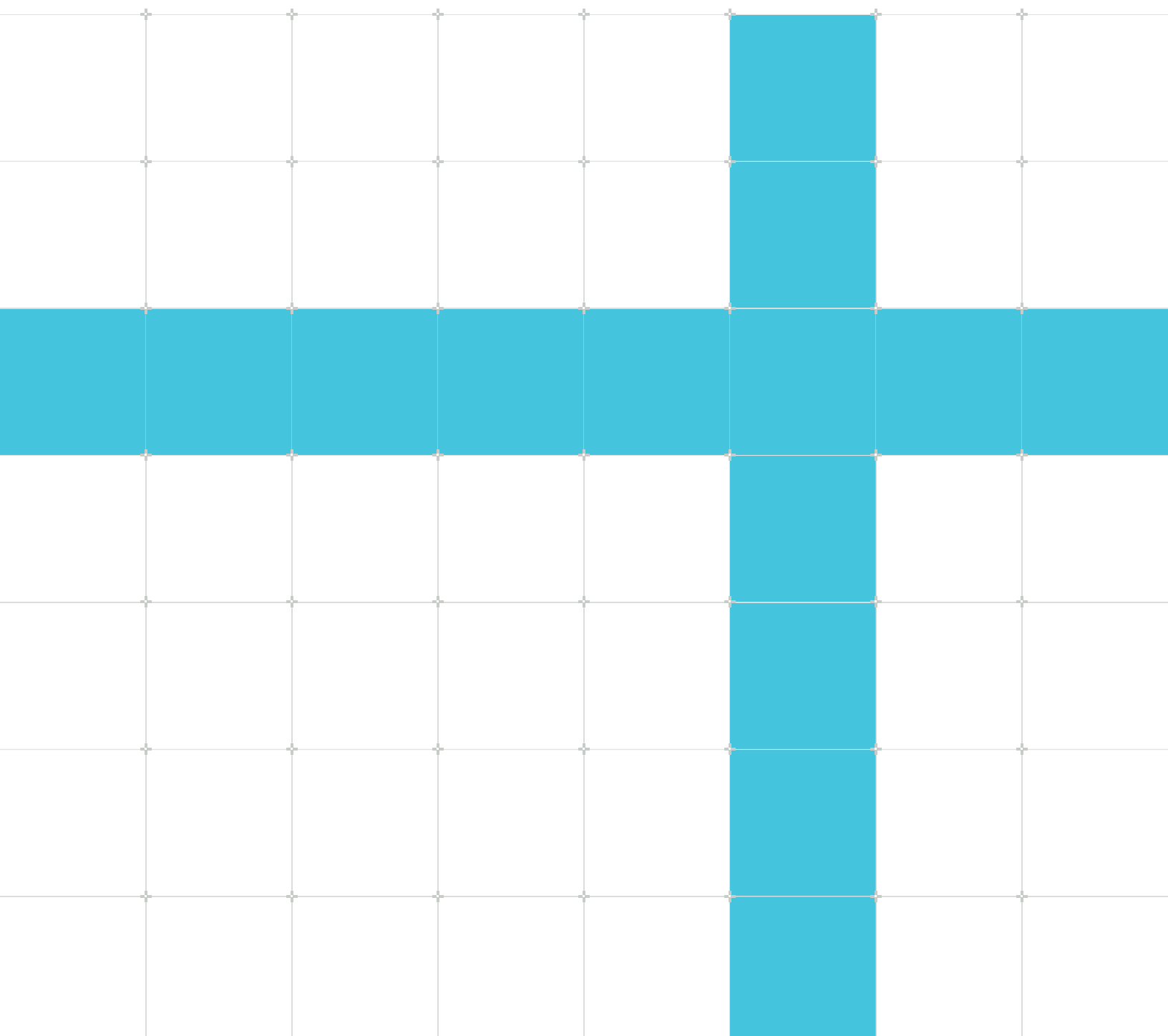
Preliminary Technical Reference Manual

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1 Introduction

1.1 Conventions

The following subsections describe conventions used in Arm documents.







1.1.1 Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm® Glossary for more information: developer.arm.com/glossary.

1.1.2 Typographic conventions

Convention	Use
<i>italic</i>	Introduces special terminology, denotes cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
monospace	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
<i>monospace italic</i>	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
monospace bold	Denotes language keywords when used outside example code.
monospace <u>underline</u>	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: <pre>MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2></pre>
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the <i>Arm Glossary</i> . For example, IMPLEMENTATION DEFINED , IMPLEMENTATION SPECIFIC , UNKNOWN , and UNPREDICTABLE .

Convention	Use
 Caution	This represents a recommendation which, if not followed, might lead to system failure or damage.
 Warning	This represents a requirement for the system that, if not followed, might result in system failure or damage.
 Danger	This represents a requirement for the system that, if not followed, will result in system failure or damage.
 Note	This represents an important piece of information that needs your attention.
 Tip	This represents a useful tip that might make it easier, better or faster to perform a task.
 Remember	This is a reminder of something important that relates to the information you are reading.

1.2 Additional reading

This document contains information that is specific to this product. See the following documents for other relevant information:

Table 1: Arm publications

Document Name	Document ID	Licensee only
AMBA® 5 CHI Architecture Specification	IHI 0050E	No
Arm® Architecture Reference Manual Supplement Morello for A-profile Architecture	DDI 0606	No
Arm® CoreLink™ CMN-600 Coherent Mesh Network Technical Reference Manual	100180	No
Arm® CoreLink™ DMC-620 Dynamic Memory Controller Technical Reference Manual	100568	No
Arm® CoreLink™ GIC-400 Generic Interrupt Controller Technical Reference Manual	DDI 0471	Yes

Document Name	Document ID	Licensee only
Arm® CoreLink™ GIC-600 Generic Interrupt Controller Technical Reference Manual	100336	Yes
Arm® CoreLink™ MMU-600 System Memory Management Unit Technical Reference Manual	100310	Yes
Arm® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual	DDI 0475	Yes
Arm® CoreLink™ TLX-400 Network Interconnect Thin Links Supplement to Arm® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual	DSU 0028	Yes
Arm® CoreSight™ Components Technical Reference Manual	DDI 0314	Yes
Arm® Cortex®-M7 Processor Technical Reference Manual	DDI 0489	Yes
Arm® DS-5 Arm DSTREAM User Guide	100955	Yes
Arm® DS-5 Debugger User Guide	100953	Yes
Arm® DS-5 Getting Started Guide	100950	Yes
Arm® Dual-Timer (SP804) Technical Reference Manual	DDI 0271	Yes
Arm® DynamIQ™ Shared Unit Technical Reference Manual	100453	Yes
Arm® Morello FVP Reference Guide Version 1.0	102225	No
Arm® Neoverse™ N1 System Development Platform Technical Reference Manual	101489	No
Arm® Power Policy Unit Architecture Specification	DEN 0051E	No
Arm® PrimeCell General Purpose Input/Output (PL061) Technical Reference Manual	DDI 0190	Yes
Arm® PrimeCell Real Time Clock (PL031) Technical Reference Manual	DDI 0224	Yes
Arm® PrimeCell System Controller SP810 Technical Reference Manual	DDI 0254	Yes
Arm® PrimeCell UART(PL011) Technical Reference Manual	DDI 0183	Yes
Arm® Watchdog Module (SP805) Technical Reference Manual	DDI 0270	Yes

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- The number 102278_0000_02_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.



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1.4 Other information

See the Arm website for other relevant information.

- [Arm® Developer](#)
- [Arm® Documentation](#)

- [Technical Support](#)
- [Arm® Glossary](#)

2 Overview

The Morello System Development Platform (SDP) is a prototype development board that contains a Morello System-on-Chip (SoC). The SDP serves as the DSbD technology platform prototype for the Morello architecture. This architecture introduces capabilities defined in the Capability Hardware Enhanced RISC Instructions (CHERI) model.

Capabilities are introduced to the Arm v8-A architecture profile as an extension of the Arm v8 AArch64 state, with the principles proposed in version 8 of the CHERI Instruction-Set Architecture (ISA), to provide hardware support for fine grain protection, and building blocks for secure, scalable compartmentalization. For more information on the A-profile capability architecture, see the *Arm® Architecture Reference Manual Supplement Morello for A-profile Architecture*.

2.1 About the Morello SDP

The Morello SDP SoC contains:

- Two CHERI-extended dual-core, out-of-order superscalar ARMv8-A-based Rainier clusters.
- CHERI-extended CMN-Skeena coherent interconnect.
- Two CHERI-extended DMC-Bing memory controllers.
- Arm Mali™-G76 Graphics Processing Unit (GPU).
- Arm Mali™ D35 Display Processing Unit (DPU).

CMN-Skeena, a coherent memory interconnect, has been designed to carry capability tag bits. Morello has two on-chip memory controllers, DMC-Bing, which support memory tagging in two different implementations:

- Client mode: A tag controller and tag cache hold memory tags.
- Server mode: ECC bits hold memory tags.

For further information, see [CMN-Skeena](#) and [DMC-Bing](#).

The purpose of Morello SDP is to:

- Target long-standing cyber-security vulnerabilities.
- Enable industrial evaluation of the CHERI-extended hardware.
- Enable software development.
- Drive a step change for industry.
- Gather evidence for adoption.

- Support ongoing research and development into the effectiveness of the Capabilities protection model.

Fixed Virtual Platform

This Preliminary Technical Reference Manual (TRM) supports the pre-silicon Fixed Virtual Platform (System Model) of Morello.

A Fixed Virtual Platform (FVP) enables the development of software without the requirement for the prototype hardware. Arm FVP models use binary translation technology to deliver fast simulations of the Arm-based system. The Morello FVP provides a functionally accurate model of the Morello SoC IP implementation, including:

- Functional register level modeling
- Hardware alignment for memory and interrupt maps, and system architecture.

The FVP model does not provide:

- Timing and cycle count information
- Lower-level peripheral component interactions
- Other hardware specific behavior

For a detailed description along with information on how to download, install and verify the FVP, see the *Arm® Morello FVP Reference Guide Version 1.0*.

A full Morello SDP TRM is planned for the physical board release in 2021. The full release will include all the necessary information, component interactions and hardware descriptions that are not described in this Preliminary TRM.



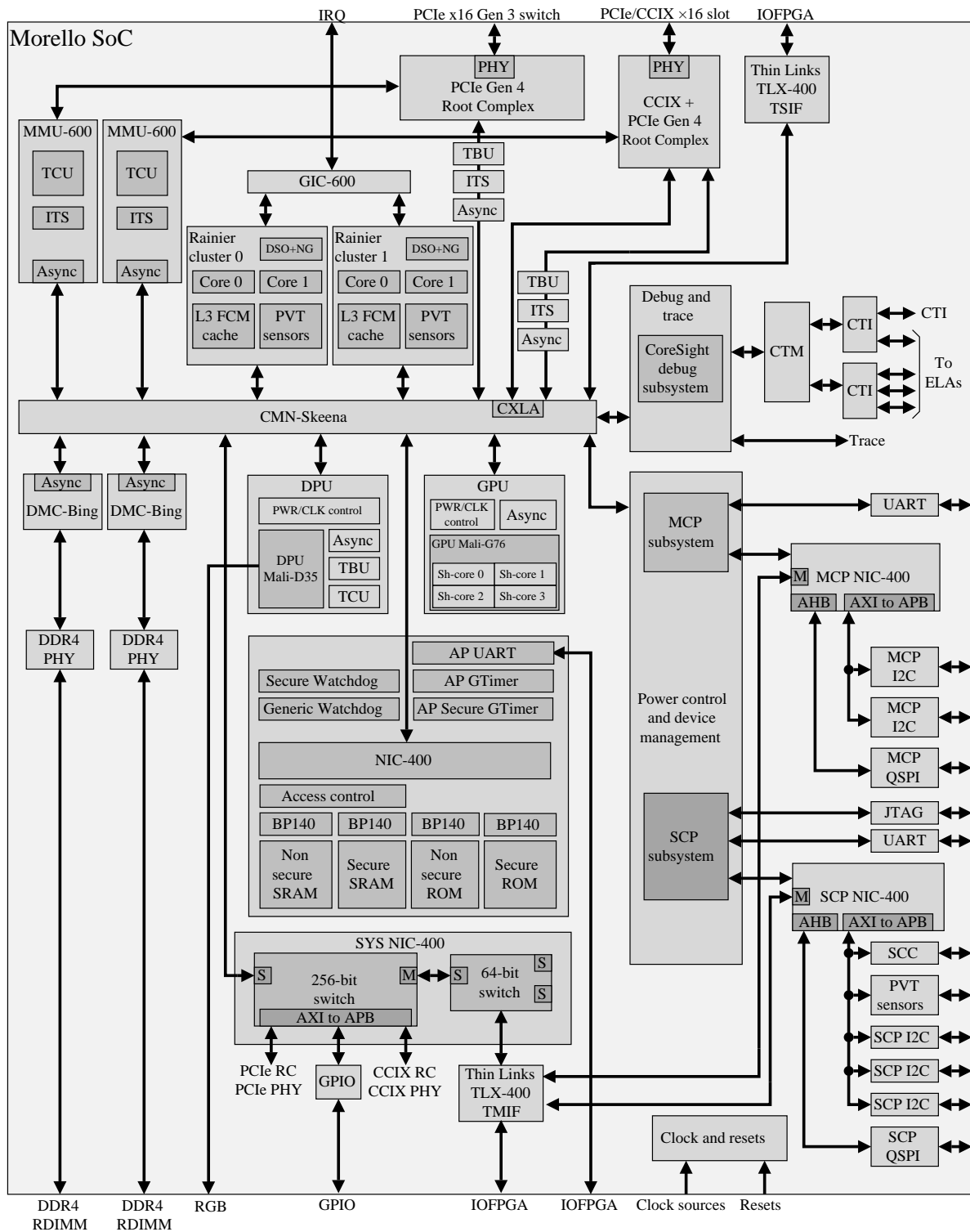
Note

The Morello SDP board is closely based on the Arm® Neoverse™ N1 System Development Platform board. To gain insight into component interactions and hardware descriptions that are not described in this Preliminary TRM, see the *Arm® Neoverse™ N1 System Development Platform Technical Reference Manual*.

3 Hardware description

The following figure shows a high-level view of architecture of the Morello SoC.

Figure 1: Morello SoC





The Morello SDP board is closely based on the Arm® Neoverse™ N1 System Development Platform board. To gain insight into component interactions and hardware descriptions that are not described in this Preliminary TRM, see the *Arm® Neoverse™ N1 System Development Platform Technical Reference Manual*.

3.1 Major components of the Morello SoC

The Morello SoC contains the following components and interfaces:

- Two dual-core Rainier clusters. Each cluster has:
 - 64KB private L1 instruction cache for each core.
 - 64KB private L1 data cache for each core.
 - 1MB private L2 unified cache for each core.
 - 1MB shared L3 unified cache in the DynamIQ™ Shared Unit (DSU) Flash Cache Module (FCM).
 - Digital Storage Oscilloscope (DSO) for voltage sensing and logic monitoring, with current stimulus generated by a separate Noise Generator (NG).
- CMN-Skeena interconnect with Coherent Multichip Link (CML):
 - Runs from **INTPLLCLK** default 1.6GHz.
 - 1GHz clock, **CXSCLK** for CCIX block in CMN-Skeena interconnect.



Arm recommends that you set the CMN-Skeena clock, **INTPLLCLK**, to 1.5GHz maximum using the SCC registers. See [Clock programming and control](#), [INT_PLL_CTRL0 Register](#), and [INT_PLL_CTRL1 Register](#).

- Embedded Logic Analyzer (ELA) on the Rainier cores and FCM DSU.
- Base element:
 - Secure region: 512KB RAM, 128KB ROM.
 - Non-secure region: 64KB RAM, 4KB ROM.
- GIC-600 (GICv3).
- MMU-600 Memory Management Units.
- Cortex®-M7 based internal System Control Processor (SCP) and Manageability Control Processor (MCP):
 - Secure boot, power management, and device management.
- CoreSight™ debug and trace.
- One Cache-Coherent Interconnect for Accelerators (CCIX) Gen 4 Root Complex and PHY:
 - Connects to one ×16 PCI Express slot.

- One PCIe Gen 4 Root Complex and PHY, running as Gen 3. Connects to the following downstream slots and peripherals through a PCI Express Gen 3 switch:
 - One ×16 PCI Express slot.
 - One ×8 PCI Express slot.
 - One ×1 PCI Express slot.
 - One ×1 Gigabit Ethernet controller.
 - One ×1 SATA 3 controller.
 - One ×1 USB 3 controller.
- Master and slave Thin Links (TLX-400) interfaces:
 - Low speed peripheral in on-board IOFPGA.
- Two 72-bit DMC-Bing DDR4 controllers:
 - Support for one 288-pin RDIMM DDR4 per interface. Up to DDR4-2667 speed.
 - Support for Tag Cache.
- Interfaces for AP, SCP, and MCP, routed to the Platform Controller Chip (PCC) on the board:
 - Four UART (PL011) interfaces.
 - Three I2C for SCP and two I2C interfaces for MCP.
 - Two QSPI interfaces: bootup for SCP and bootup for MCP.
- 8-bit GPIO (PL061) for on-board I/O.
- Serial Configuration Controller (SCC) interface to IOFPGA.
- Process, Voltage, and Temperature (PVT) sensors.
- 32-bit Mobile Industry Process Interface (MIPI-60) Trace port.
- JTAG debug port.
- Arm Mali™-G76 Graphics Processing Unit (GPU):
 - Four shader cores.
 - Support enabled for Arm Frame Buffer Compression (AFBC).
- Arm Mali™ D35 Display Processor Unit (DPU):
 - Single HDMI 1.4a display output.
 - Support for UXGA 1600 x 1200 resolution.

For further information about the Rainier clusters, CMN-Skeena, and DMC-Bing, see:

- [Rainier clusters](#)
- [CMN-Skeena](#)
- [DMC-Bing](#)

3.2 Clock programming and control

The System Configuration Control (SCC) clock control registers in the Morello SoC control the clock frequencies by modifying the clock PLLs and dividers.

The PLLs generate the internal clocks from the board OSC clock generators according to the formula:

Output clock frequency = (Input clock frequency/REFDIV)×FBDIV/POSTDIV where:

- REFDIV is input frequency division value.
- FBDIV is the PLL feedback division value.
- POSTDIV is the PLL output frequency division value.

The SCC PLL control registers set the values REFDIV, FBDIV, and POSTDIV for each PLL. Other SCC registers control the clock dividers and select the inputs for the internal clocks.

The following table shows the SCC clock control registers.

Table 2: SCC clock control registers

Register	Register function	Register description
PMCLK_DIV	Sets value of divider value to generate PMCLK from REFCLK .	See PMCLK_DIV Register .
SYSAPBCLK_CTRL	Selects input clock to generate SYSAPBCLK .	See SYSAPBCLK_CTRL Register .
SYSAPBCLK_DIV	Sets value of divider value to generate SYSAPBCLK from SYSPLLCLK .	See SYSAPBCLK_DIV Register .
TMIF2XCLK_CTRL	Selects input clock to generate TMIF2XCLK .	See IOFPGA_TMIF2XCLK_CTRL Register .
TMIF2XCLK_DIV	Sets value of divider value to generate TMIF2XCLK from SYSPLLCLK .	See IOFPGA_TMIF2XCLK_DIV Register .
TSIF2XCLK_CTRL	Selects input clock to generate TSIF2XCLK .	See IOFPGA_TSIF2XCLK_CTRL Register .
TSIF2XCLK_DIV	Sets value of divider value to generate TSIF2XCLK from SYSPLLCLK .	See IOFPGA_TSIF2XCLK_DIV Register .
SCPNICCLK_CTRL	Selects input clock to generate SCPNICCLK .	See SCPNICCLK_CTRL Register .
SCPNICCLK_DIV	Sets value of divider value to generate SCPNICCLK from SYSPLLCLK .	See SCPNICCLK_DIV Register .

Register	Register function	Register description
SCPI2CCLK_CTRL	Selects input clock to generate SCPI2CCLK .	See SCPI2CCLK_CTRL Register .
SCPI2CCLK_DIV	Sets value of divider value to generate SCPI2CCLK from SYSPLLCLK .	See SCPI2CCLK_DIV Register .
SCPQSPICLK_CTRL	Selects input clock to generate SCPQSPICLK .	See SCPQSPICLK_CTRL Register .
SCPQSPICLK_DIV	Sets value of divider value to generate SCPQSPICLK from SYSPLLCLK .	See SCPQSPICLK_DIV Register .
SENSORCLK_CTRL	Selects input clock to generate SENSORCLK .	See SENSORCLK_CTRL Register .
SENSORCLK_DIV	Sets value of divider value to generate SENSORCLK from SYSPLLCLK .	See SENSORCLK_DIV Register .
MCPNICCLK_CTRL	Selects input clock to generate MCPNICCLK .	See MCPNICCLK_CTRL Register .
MCPNICCLK_DIV	Sets value of divider value to generate MCPNICCLK from SYSPLLCLK .	See MCPNICCLK_DIV Register .
MCPI2CCLK_CTRL	Selects input clock to generate MCPI2CCLK .	See MCPI2CCLK_CTRL Register .
MCPI2CCLK_DIV	Sets value of divider value to generate MCPI2CCLK from SYSPLLCLK .	See MCPI2CCLK_DIV Register .
MCPQSPICLK_CTRL	Selects input clock to generate MCPQSPICLK .	See MCPQSPICLK_CTRL Register .
MCPQSPICLK_DIV	Sets value of divider value to generate MCPQSPICLK from SYSPLLCLK .	See MCPQSPICLK_DIV Register .
PCIEAXICLK_CTRL	Selects input clock to generate PCIEAXICLK .	See PCIEAXICLK_CTRL Register .
PCIEAXICLK_DIV	Sets value of divider value to generate PCIEAXICLK from SYSPLLCLK .	See PCIEAXICLK_DIV Register .
CCIXAXICLK_CTRL	Selects input clock to generate CCIXAXICLK .	See CCIXAXICLK_CTRL Register .
CCIXAXICLK_DIV	Sets value of divider value to generate CCIXAXICLK from SYSPLLCLK .	See CCIXAXICLK_DIV Register .
PCIEAPBCLK_CTRL	Selects input clock to generate PCIEAPBCLK .	See PCIEAPBCLK_CTRL Register .
PCIEAPBCLK_DIV	Sets value of divider value to generate PCIEAPBCLK from SYSPLLCLK .	See PCIEAPBCLK_DIV Register .
CCIXAPBCLK_CTRL	Selects input clock to generate CCIXAPBCLK .	See CCIXAPBCLK_CTRL Register .

Register	Register function	Register description
CCIXAPBCLK_DIV	Sets value of divider value to generate CCIXAPBCLK from SYSPLLCLK .	See CCIXAPBCLK_DIV Register .
SYS_CLK_EN	Enables or disables internally generated clocks.	See SYS_CLK_EN Register .
CPU0_PLL_CTRL0	Controls CPU0PLL to generate CPU0PLLCLK .	See CPU0_PLL_CTRL0 Register .
CPU0_PLL_CTRL1	Controls CPU0PLL to generate CPU0PLLCLK .	See CPU0_PLL_CTRL1 Register .
CPU1_PLL_CTRL0	Controls CPU1PLL to generate CPU1PLLCLK .	See CPU1_PLL_CTRL0 Register .
CPU1_PLL_CTRL1	Controls CPU1PLL to generate CPU1PLLCLK .	See CPU1_PLL_CTRL1 Register .
CLUS_PLL_CTRL0	Controls CLUSPLL to generate CLUSPLLCLK .	See CLUS_PLL_CTRL0 Register .
CLUS_PLL_CTRL1	Controls CLUSPLL to generate CLUSPLLCLK .	See CLUS_PLL_CTRL1 Register .
SYS_PLL_CTRL0	Controls SYSPLL to generate SYSPLLCLK .	See SYS_PLL_CTRL0 Register .
SYS_PLL_CTRL1	Controls SYSPLL to generate SYSPLLCLK .	See SYS_PLL_CTRL1 Register .
DMC_PLL_CTRL0	Controls DMCPLL to generate DMCPLLCLK .	See DMC_PLL_CTRL0 Register .
DMC_PLL_CTRL1	Controls DMCPLL to generate DMCPLLCLK .	See DMC_PLL_CTRL1 Register .
INT_PLL_CTRL0	Controls INTPLL to generate INTPLLCLK .	See INT_PLL_CTRL0 Register .
INT_PLL_CTRL1	Controls INTPLL to generate INTPLLCLK .	See INT_PLL_CTRL1 Register .
GPU_PLL_CTRL0	Controls GPUPLL to generate GPUPLLCLK .	See GPU_PLL_CTRL0 Register .
GPU_PLL_CTRL1	Controls GPUPLL to generate GPUPLLCLK .	See GPU_PLL_CTRL1 Register .
DPU_PLL_CTRL0	Controls DPUPLL to generate DPUPLLCLK .	See DPU_PLL_CTRL0 Register .
DPU_PLL_CTRL1	Controls DPUPLL to generate DPUPLLCLK .	See DPU_PLL_CTRL1 Register .
PXL_PLL_CTRL0	Controls PXLPLL to generate PXLPLLCLK .	See PXL_PLL_CTRL0 Register .
PXL_PLL_CTRL1	Controls PXLPLL to generate PXLPLLCLK .	See PXL_PLL_CTRL1 Register .

3.3 PCI Express and CCIX systems

The Morello SDP provides PCI Express Gen 4, and Cache-Coherent Interconnect for Accelerators (CCIX) expansion.

3.3.1 Overview of PCIe and CCIX systems

The Morello SoC provides two PCI Express Gen 4 x16, 16Gbps, independent interfaces. One of the interfaces supports Cache-Coherent Interconnect for Accelerators (CCIX) technology. CCIX has two functions:

- CCIX acceleration.
- Multi socket operation.

For multi socket operation, the Morello SoC and board provide the Chip to Chip (C2C) sideband signals necessary for CCIX expansion. The CCIX interface also functions as a standard PCIe Gen 4 interface.

One Gen 4 Root Complex on the Morello SoC connects directly to a Gen 3 switch. Downstream of the switch provides access to three PCIe slots, a four-port USB 3.0 Host Controller, a two-port SATA controller, and one Gigabit Ethernet port.

The other Gen 4 Root Complex on the Morello SoC provides access through one x16 CCIX slot which also functions as a standard PCIe Gen 4 interface.

The GbE, USB 3.0, and C2C connectors are accessible on the back panel. The PCIe and CCIX slots, and the SATA ports, are accessible by removing the side panel.

3.3.2 SATA 3.0 ports

The PCIe switch connects to the SATA 3.0 controller over a x1 PCIe link.

The SATA 3.0 controller drives two SATA 3.0 ports for hard drives:

- The SATA 3.0 is a Marvell 88SE9170 SATA 3.0 controller with a x1 Gen 2 link to the PCIe switch.
- The connections between the SATA 3.0 ports and the SATA 3.0 controller have a Serial ATA Generation 3 transfer rate of 6Gbps.

3.3.3 Gigabit Ethernet port

The PCIe switch connects to the Gigabit Ethernet (GbE) controller over a ×1 Gen 1.1 link.

The GbE controller drives an RJ45 GbE port on the back panel.

- The GbE controller is a RealTek RTL8111GS device.
- The controller provides a 10/100/1000Base-T connection to the GbE port.

3.4 UARTs

The Morello SDP UART system enables access to the Morello SoC.

Morello SoC provides:

- AP0 UART - Non-secure application processor UART.
- AP2 UART - Secure application processor UART.
- SCP UART - System Control Processor UART.
- MCP UART - Manageability Control Processor UART.

AP2 UART

Morello provides an additional secure UART for applications processors. AP2 UART features:

- PL011 UART.
- APB3 interface.
- Transmit and receive FIFOs with 32 entries.
- 8-bit words.

4 Programmers model

This chapter describes the programmers model of the Morello SDP.

4.1 About this programmers model

The following information applies to all registers in this programmers model:

- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in UNPREDICTABLE behavior.
- Unless otherwise stated in the accompanying text:
 - Do not modify undefined register bits.
 - Ignore undefined register bits on reads.
 - All register bits are reset to a logic 0 by a system or powerup reset.
 - All register summary tables in this chapter describe register access types as follows:

RW

Read/write.

RO

Read-only.

WO

Write-only.

4.2 Morello SDP memory maps

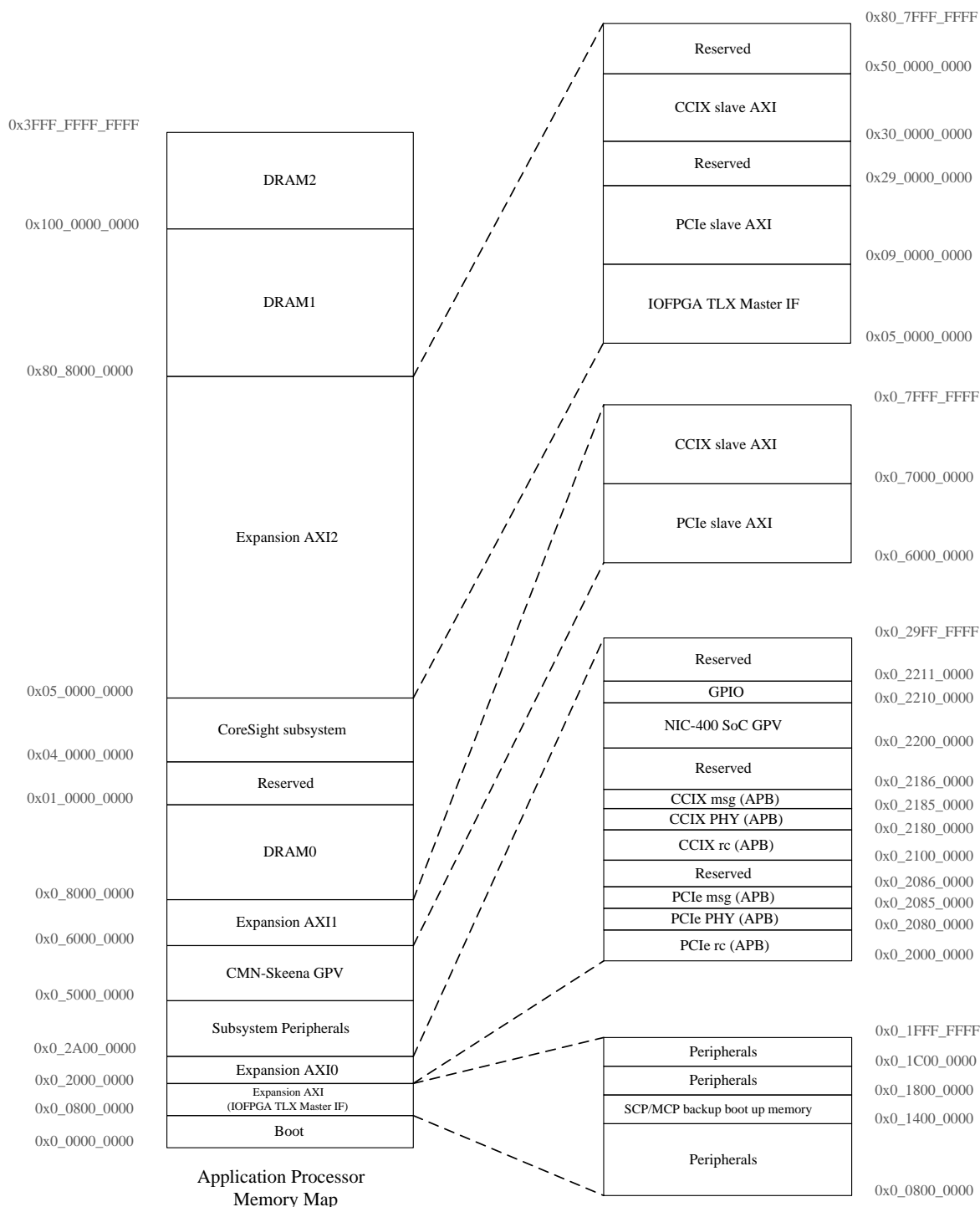
The Morello SDP contains Application Processor (AP), System Control Processor (SCP), and Manageability Control Processor (MCP) memory maps.

The SCP and MCP memory maps are private. The masters which can access the AP memory map have no access to the components in the SCP and MCP memory maps. Certain areas within the AP memory map are mapped into the SCP and MCP memory maps and the corresponding masters can access them.

4.2.1 Application Processor memory map

The following figure shows the Morello SDP Application Processor (AP) memory map.

Figure 2: AP memory map



The following table shows the Morello SDP AP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 3: SDP AP memory map

Address range from	Address range to	Size	Description
0x0_0000_0000	0x0_07FF_FFFF	128MB	Boot region
0x0_0800_0000	0x0_13FF_FFFF	192MB	Peripherals
0x0_1400_0000	0x0_17FF_FFFF	64MB	SCP, MCP backup boot memory
0x0_1800_0000	0x0_1BFF_FFFF	64MB	Peripherals
0x0_1C00_0000	0x0_1FFF_FFFF	64MB	Peripherals
0x0_2000_0000	0x0_207F_FFFF	8MB	PCIe rc (APB)
0x0_2080_0000	0x0_2084_FFFF	320KB	PCIe PHY (APB)
0x0_2085_0000	0x0_2085_FFFF	64KB	PCIe msg (APB)
0x0_2100_0000	0x0_217F_FFFF	8MB	CCIX rc (APB)
0x0_2180_0000	0x0_2184_FFFF	320KB	CCIX PHY (APB)
0x0_2185_0000	0x0_2185_FFFF	64KB	CCIX msg (APB)
0x0_2200_0000	0x0_220F_FFFF	1MB	NIC-400 SoC GPV
0x0_2210_0000	0x0_2210_FFFF	64KB	GPIO
0x0_2A00_0000	0x0_4FFF_FFFF	608MB	Subsystem peripherals
0x0_5000_0000	0x0_5FFF_FFFF	256MB	CMN-Skeena GPV
0x0_6000_0000	0x0_6FFF_FFFF	256MB	PCIe slave AXI
0x0_7000_0000	0x0_7FFF_FFFF	256MB	CCIX slave AXI
0x0_8000_0000	0x0_FFFF_FFFF	2GB	DRAM0
0x4_0000_0000	0x4_FFFF_FFFF	4GB	CoreSight subsystem
0x5_0000_0000	0x8_FFFF_FFFF	16GB	IOFPGA TLX Master IF

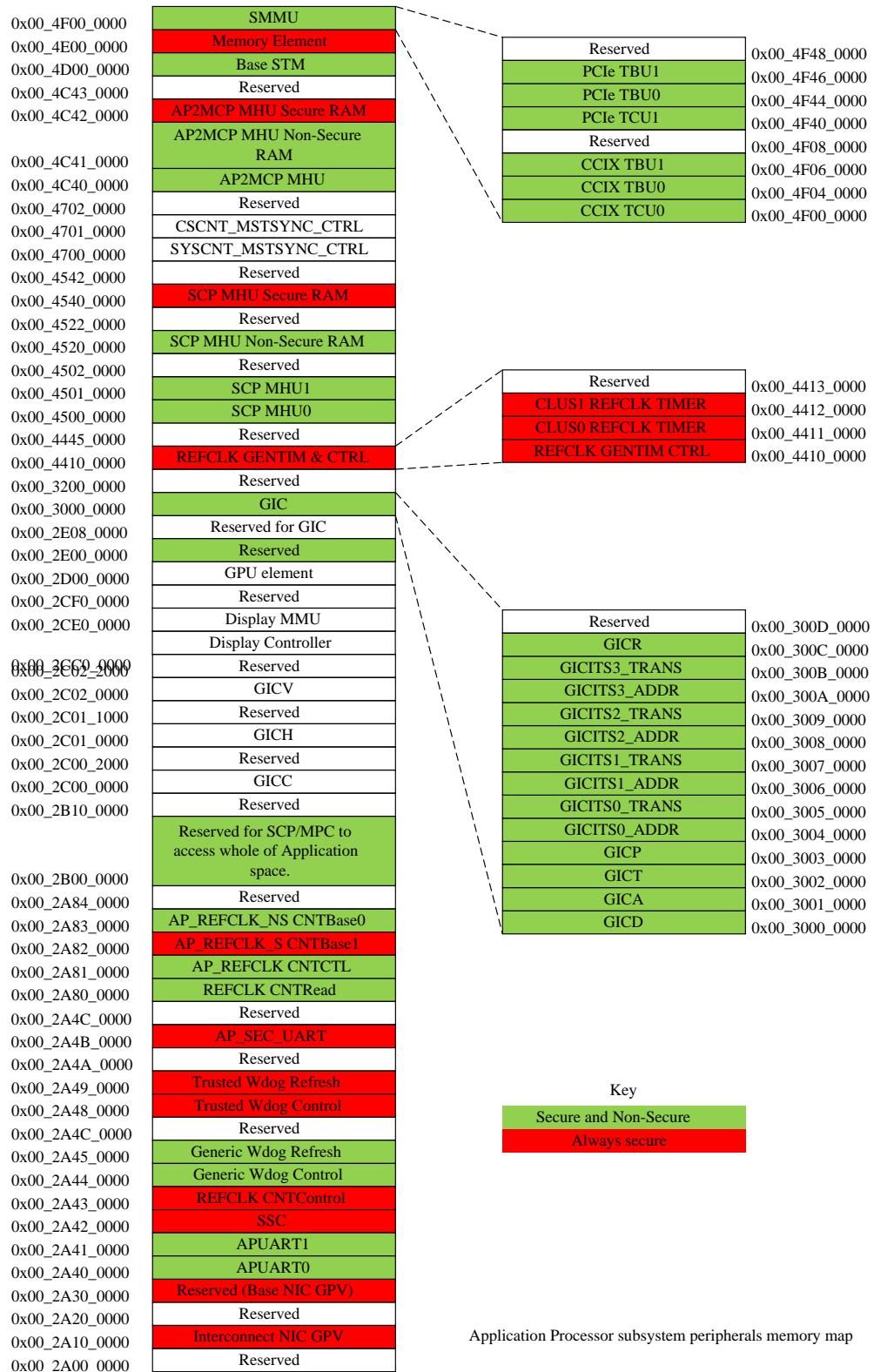
Address range from	Address range to	Size	Description
0x9_0000_0000	0x28_FFFF_FFFF	128GB	PCIe slave AXI
0x30_0000_0000	0x4F_FFFF_FFFF	128GB	CCIX slave AXI
0x80_0000_0000	0xFF_FFFF_FFFF	510GB	DRAM1
0x100_0000_0000	0x3FF_FFFF_FFFF	3TB	DRAM2

4.2.2 Application Processor subsystem peripherals memory map

The Application Processor (AP) memory map of the Morello SDP contains a region associated with the subsystem peripherals.

The following figure shows the subsystem peripherals region of the AP memory map.

Figure 3: Subsystem peripherals region of Application Processor memory map



The following table shows the subsystem peripherals region of the AP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 4: Subsystem peripherals region of the AP memory map

Address range from	Address range to	Size	Description
0x00_2A00_0000	0x00_2A0F_FFFF	1MB	Reserved
0x00_2A10_0000	0x00_2A1F_FFFF	1MB	Interconnect NIC GPV
0x00_2A30_0000	0x00_2A3F_FFFF	1MB	Reserved (Base NIC GPV)
0x00_2A40_0000	0x00_2A40_FFFF	64KB	APUART0
0x00_2A41_0000	0x00_2A41_FFFF	64KB	APUART1
0x00_2A42_0000	0x00_2A42_FFFF	64KB	SSC
0x00_2A43_0000	0x00_2A43_FFFF	64KB	REFCLK CNTControl
0x00_2A44_0000	0x00_2A44_FFFF	64KB	Generic Watchdog Control
0x00_2A45_0000	0x00_2A45_FFFF	64KB	Generic Watchdog Refresh
0x00_2A48_0000	0x00_2A48_FFFF	64KB	Trusted Watchdog Control
0x00_2A49_0000	0x00_2A49_FFFF	64KB	Trusted Watchdog Refresh
0x00_2A4B_0000	0x00_2A4B_FFFF	64KB	AP_SEC_UART
0x00_2A80_0000	0x00_2A80_FFFF	64KB	REFCLK CNTRead
0x00_2A81_0000	0x00_2A81_FFFF	64KB	AP_REFCLK CNTCTL
0x00_2A82_0000	0x00_2A82_FFFF	64KB	AP_REFCLK_S CNTBase1
0x00_2A83_0000	0x00_2A83_FFFF	64KB	AP_REFCLK_NS CNTBase0
0x00_2B00_0000	0x00_2B0F_FFFF	1MB	Reserved for SCP/MCP to access whole of application space.
0x00_2C00_0000	0x00_2C00_1FFF	8KB	GICC registers
0x00_2C01_0000	0x00_2C01_0FFF	4KB	GICH registers
0x00_2C02_0000	0x00_2C02_1FFF	8KB	GICV registers

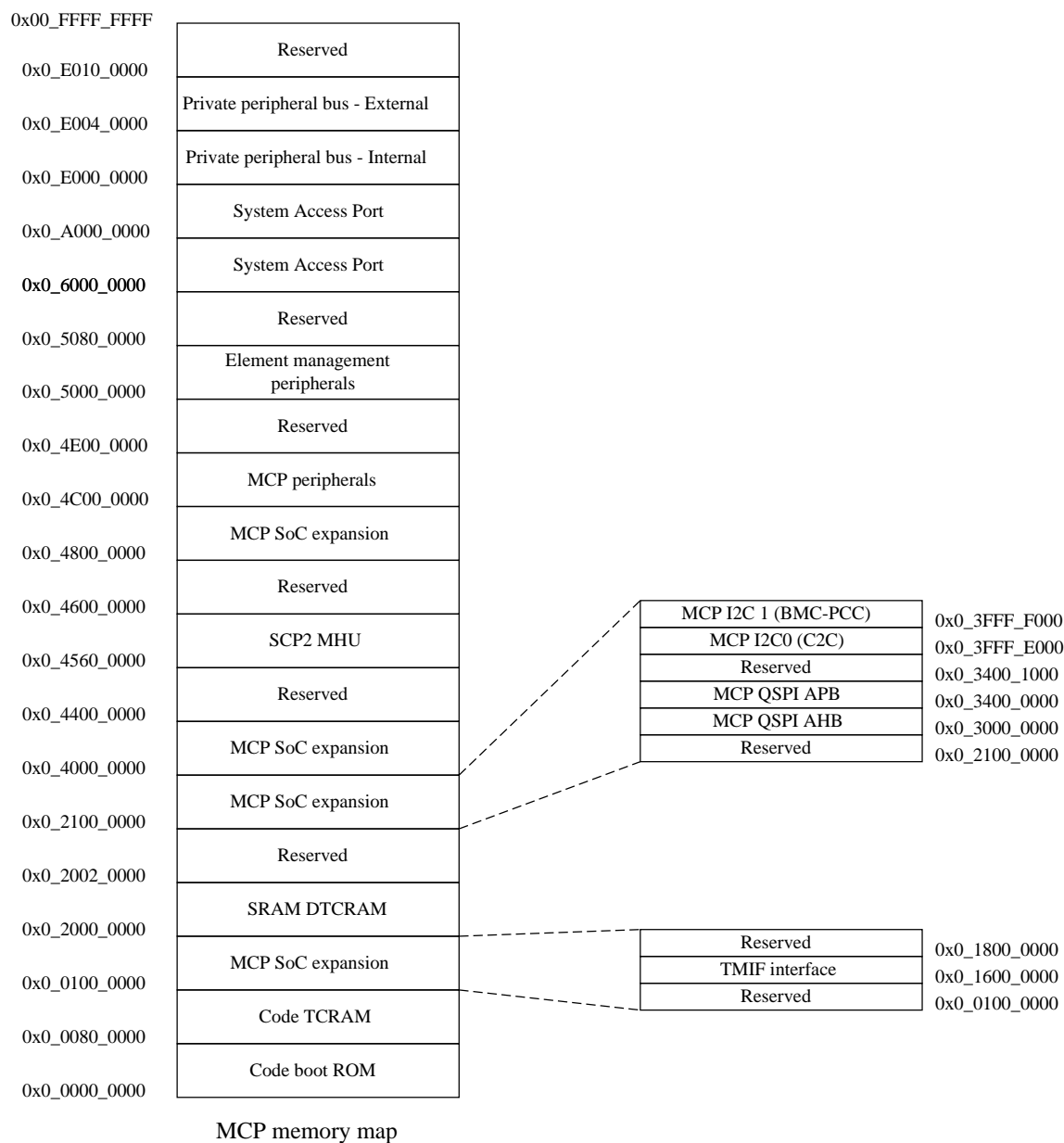
Address range from	Address range to	Size	Description
0x00_2CC0_0000	0x00_2CDF_FFFF	2MB	Display Controller
0x00_2CE0_0000	0x00_2CEF_FFFF	1MB	Display MMU
0x00_2D00_0000	0x00_2DFF_FFFF	16MB	GPU Element
0x00_2E08_0000	0x00_2FFF_FFFF	32MB	Reserved for GIC
0x00_3000_0000	0x00_3000_FFFF	64KB	GICD registers
0x00_3001_0000	0x00_3001_FFFF	64KB	GICA registers
0x00_3002_0000	0x00_3002_FFFF	64KB	GICT registers
0x00_3003_0000	0x00_3003_FFFF	64KB	GICP registers
0x00_3004_0000	0x00_3004_FFFF	64KB	GICITS0 ITS address
0x00_3005_0000	0x00_3005_FFFF	64KB	GICITS0 translator
0x00_3006_0000	0x00_3006_FFFF	64KB	GICITS1 address
0x00_3007_0000	0x00_3007_FFFF	64KB	GICITS1 translator
0x00_3008_0000	0x00_3008_FFFF	64KB	GICITS2 address
0x00_3009_0000	0x00_3009_FFFF	64KB	GICITS2 translator
0x00_300A_0000	0x00_300A_FFFF	64KB	GICITS3 address
0x00_300B_0000	0x00_300B_FFFF	64KB	GICITS3 address
0x00_300C_0000	0x00_300C_FFFF	64KB	GICR registers
0x00_4410_0000	0x00_4410_FFFF	64KB	REFCLK general timer control
0x00_4411_0000	0x00_4411_FFFF	64KB	Cluster 0 time frame
0x00_4412_0000	0x00_4412_FFFF	64KB	Cluster 1 time frame
0x00_4500_0000	0x00_4500_FFFF	64KB	SCP Message Handling Unit0(MHU0)
0x00_4501_0000	0x00_4501_FFFF	64KB	SCP MHU1

Address range from	Address range to	Size	Description
0x00_4520_0000	0x00_4521_FFFF	128KB	SCP MHU Non-secure RAM
0x00_4540_0000	0x00_4541_FFFF	128KB	SCP MHU Secure RAM
0x00_4700_0000	0x00_4700_FFFF	64KB	SYSCNT_MSTSYN_CTRL
0x00_4701_0000	0x00_4701_FFFF	64KB	CSCNT_MSTSYNC_CTRL
0x00_4C40_0000	0x00_4C40_FFFF	64KB	AP2MCP MHU
0x00_4C41_0000	0x00_4C41_FFFF	64KB	AP2MCP MHU Non-Secure RAM
0x00_4C42_0000	0x00_4C42_FFFF	64KB	AP2MCP MHU Secure RAM
0x00_4D00_0000	0x00_4DFF_FFFF	16MB	Base STM
0x00_4E00_0000	0x00_4EFF_FFFF	16MB	Memory Element
0x00_4F00_0000	0x00_4F03_FFFF	256KB	Translation Control Unit0 (TCU0) for CCIX root port.
0x00_4F04_0000	0x00_4F05_FFFF	128KB	Translation Buffer Unit0 (TBU0) for CCIX root port.
0x00_4F06_0000	0x00_4F07_FFFF	128KB	Translation Buffer Unit1 (TBU1) for CCIX root port.
0x00_4F40_0000	0x00_4F43_FFFF	256KB	Translation Control Unit1 (TCU0) for PCIe root port.
0x00_4F44_0000	0x00_4F45_FFFF	128KB	Translation Buffer Unit0 (TBU0) for PCIe root port.
0x00_4F46_0000	0x00_4F47_FFFF	128KB	Translation Buffer Unit1 (TBU1) for PCIe root port.

4.2.3 Manageability Control Processor memory map

The following figure shows the Morello SDP Manageability Control Processor (MCP) memory map.

Figure 4: MCP memory map



The following table shows the Morello SDP MCP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 5: MCP memory map

Address range From	Address range To	Size	Description
0x0_0000_0000	0x0_007F_FFFF	8MB	Code boot ROM
0x0_0080_0000	0x0_00FF_FFFF	8MB	Code TCRAM
0x0_0100_0000	0x0_15FF_FFFF	336MB	Reserved part of MCP SoC expansion memory
0x0_1600_0000	0x0_17FF_FFFF	32MB	TMIF interface
0x0_1800_0000	0x0_1FFF_FFFF	128MB	Reserved part of MCP SoC expansion memory
0x0_2000_0000	0x0_20FF_FFFF	16MB	SRAM DTCRAM
0x0_2100_0000	0x0_2FFF_FFFF	240MB	Reserved part of MCP SoC expansion memory
0x0_3000_0000	0x0_33FF_FFFF	64MB	MCP QSPI AHB
0x0_3400_0000	0x0_3400_0FFF	4KB	MCP QSPI APB
0x0_3400_1000	0x0_3FFF_DFFF	191MB	Reserved part of MCP SoC expansion memory
0x0_3FFF_E000	0x0_3FFF_EFFF	4KB	MCP I2C0 (C2C)
0x0_3FFF_F000	0x0_3FFF_FFFF	4KB	MCP I2C 1 (BMC-PCC)
0x0_4000_0000	0x0_43FF_FFFF	64MB	MCP SoC expansion
0x0_4400_0000	0x0_455F_FFFF	22MB	Reserved
0x0_4560_0000	0x0_45FF_FFFF	10MB	SCP2 MHU
0x0_4600_0000	0x0_47FF_FFFF	32MB	Reserved
0x0_4800_0000	0x0_4BFF_FFFF	64MB	MCP SoC expansion
0x0_4C00_0000	0x0_4DFF_FFFF	32MB	MCP peripherals
0x0_4E00_0000	0x0_4FFF_FFFF	32MB	Reserved
0x0_5000_0000	0x0_507F_FFFF	8MB	Element management peripherals

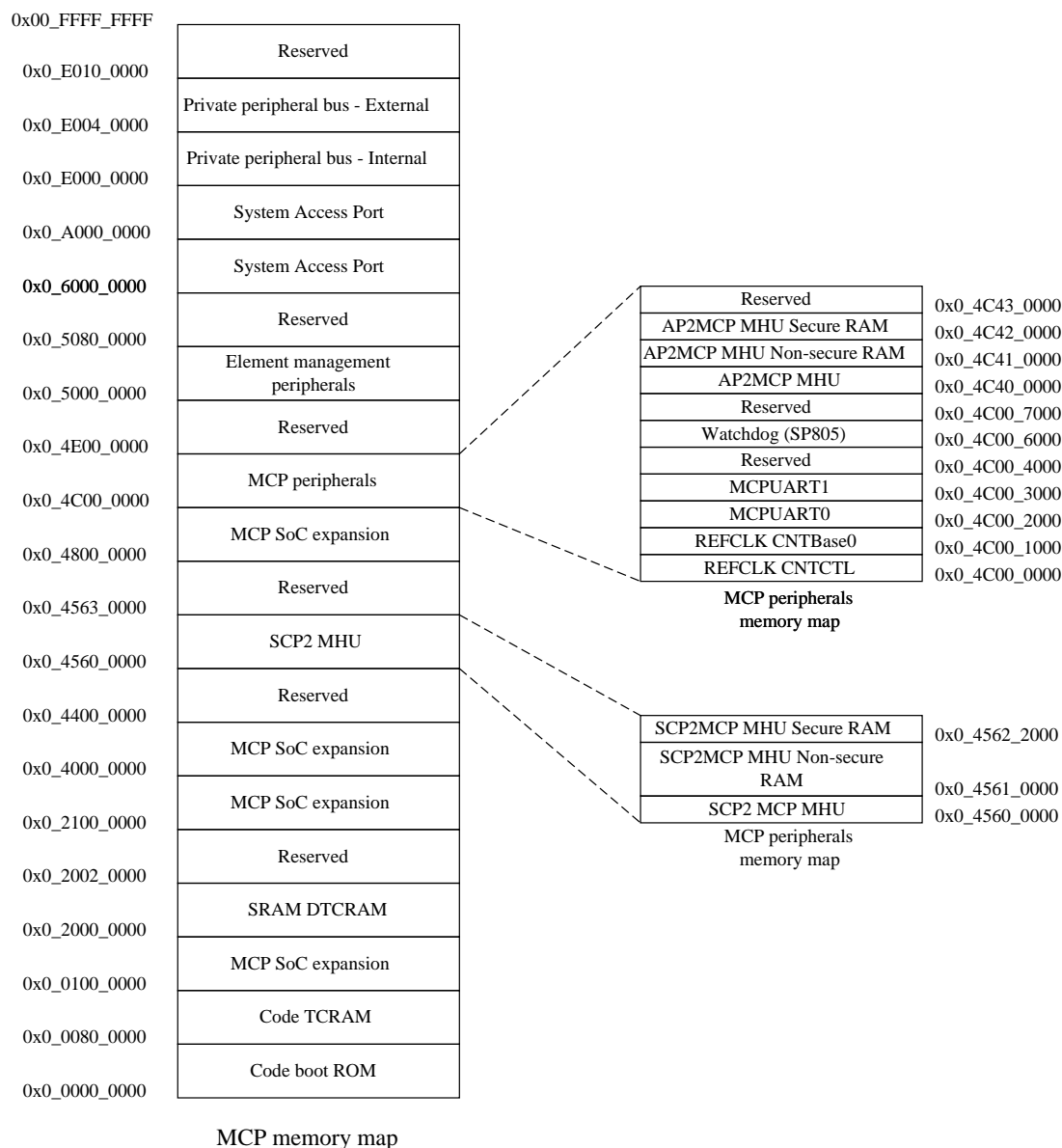
Address range From	Address range To	Size	Description
0x0_5080_0000	0x0_5FFF_FFFF	248MB	Reserved
0x0_6000_0000	0x0_9FFF_FFFF	1GB	System Access Port. Translated to 0x0_4000_0000 to 0x0_7FFF_FFFF of AP memory map.
0x0_A000_0000	0x0_DFFF_FFFF	1GB	System Access Port. Translated to 0x0_0000_0000 to 0x0_3FFF_FFFF of AP memory map with debug address translation not enabled. Translated to 0x4_0000_0000 to 0x4_3FFF_FFFF of AP memory map with debug address translation enabled.
0x0_E000_0000	0x0_E003_FFFF	256KB	Private peripheral bus - Internal.
0x0_E004_0000	0x0_E00F_FFFF	768KB	Private peripheral bus - External.
0x0_E010_0000	0x0_FFFF_FFFF	511MB	Reserved

4.2.4 Manageability Control Processor peripherals memory map

The Manageability Control Processor (MCP) memory map of the Morello SDP contains a region associated with the MCP peripherals.

The following figure shows the peripherals region of the MCP memory map.

Figure 5: MCP peripherals memory map



The following table shows the peripherals region of the MCP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

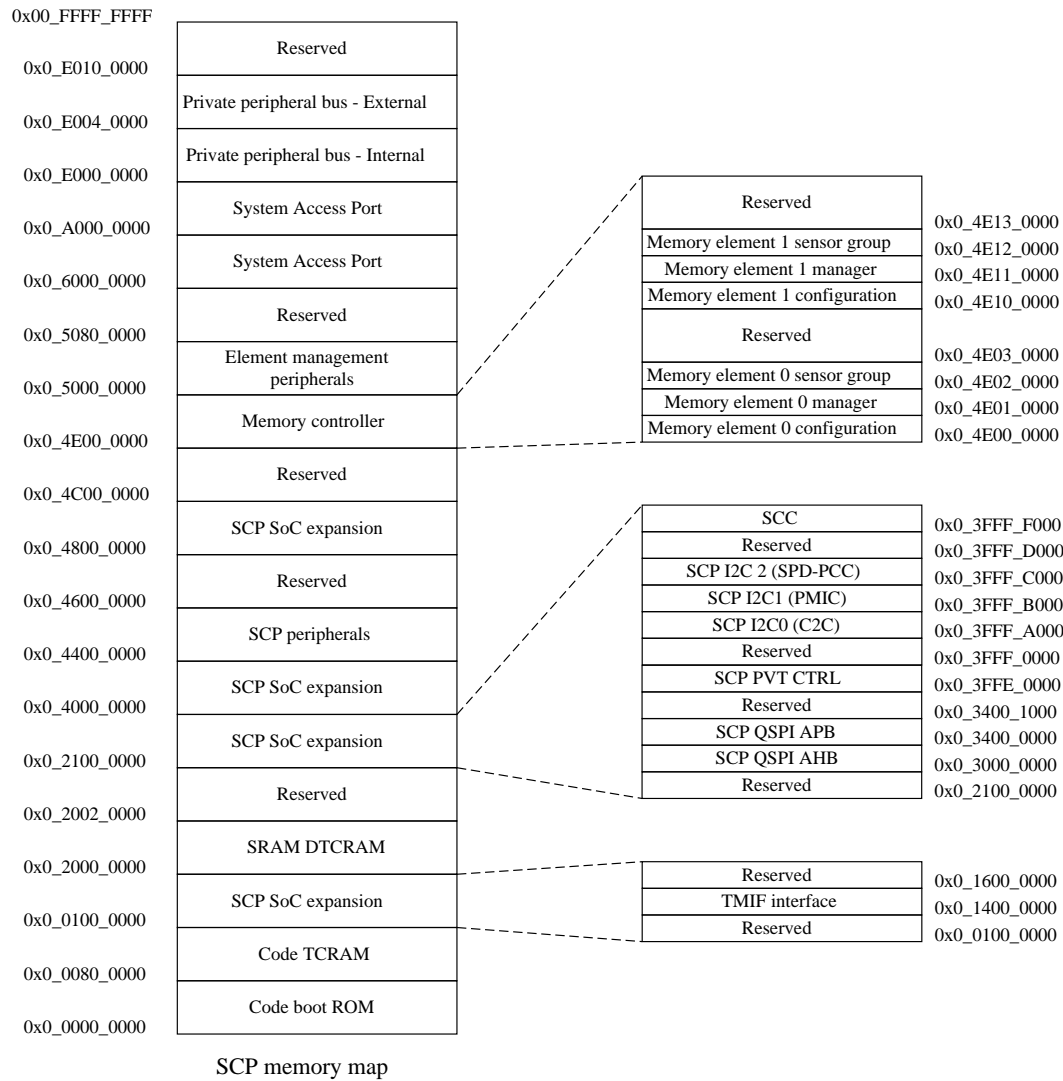
Table 6: MCP peripherals memory map

Address range From	Address range To	Size	Description
0x00_4560_0000	0x00_4560_FFFF	64KB	SCP2 MCP Message Handling Unit (MHU)
0x00_4561_0000	0x00_4561_FFFF	64KB	SCP2 MCP MHU Non-secure RAM
0x00_4562_0000	0x00_4562_FFFF	64KB	SCP2 MCP MHU Secure RAM
0x00_4C00_0000	0x00_4C00_0FFF	4KB	REFCLK CNTCTL
0x00_4C00_1000	0x00_4C00_1FFF	4KB	REFCLK CNTBase0
0x00_4C00_2000	0x00_4C00_2FFF	4KB	MCPUART0
0x00_4C00_3000	0x00_4C00_3FFF	4KB	MCPUART1
0x00_4C00_6000	0x00_4C00_6FFF	4KB	Watchdog (SP805)
0x00_4C40_0000	0x00_4C40_FFFF	64KB	AP2 MCP MHU
0x00_4C41_0000	0x00_4C41_FFFF	64KB	AP2 MCP MHU Non-secure RAM
0x00_4C42_0000	0x00_4C42_FFFF	64KB	AP2 MCP MHU Secure RAM

4.2.5 System Control Processor memory map

The following figure shows the Morello SDP System Control Processor (SCP) memory map.

Figure 6: SCP memory map



The following table shows the Morello SDP SCP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 7: SCP memory map

Address range from	Address range to	Size	Description
0x0_0000_0000	0x0_007F_FFFF	8MB	Code boot ROM
0x0_0080_0000	0x0_00FF_FFFF	8MB	Code TCRAM
0x0_0100_0000	0x0_13FF_FFFF	304MB	Reserved part of SCP SoC expansion memory
0x0_1400_0000	0x0_15FF_FFFF	32MB	TMIF interface
0x0_1600_0000	0x0_1FFF_FFFF	160MB	Reserved part of SCP SoC expansion memory
0x0_2000_0000	0x0_20FF_FFFF	16MB	SRAM DTCRAM
0x0_2100_0000	0x0_2FFF_FFFF	240MB	Reserved part of SCP SoC expansion memory
0x0_3000_0000	0x0_33FF_FFFF	64MB	SCP QSPI AHB
0x0_3400_0000	0x0_3400_0FFF	4KB	SCP QSPI APB
0x0_3400_1000	0x0_3FFD_FFFF	191MB	Reserved part of SCP SoC expansion memory
0x0_3FFE_0000	0x0_3FFE_FFFF	64KB	SCP PVT CTRL
0x0_3FFF_1000	0x0_3FFF_9FFF	40KB	Reserved part of SCP SoC expansion memory
0x0_3FFF_A000	0x0_3FFF_AFFF	4KB	SCP I2C0 (C2C)
0x0_3FFF_B000	0x0_3FFF_BFFF	4KB	SCP I2C1 (PMIC)
0x0_3FFF_C000	0x0_3FFF_CFFF	4KB	SCP I2C2 (SPD-PCC)
0x0_3FFF_D000	0x0_3FFF_EFFF	8KB	Reserved part of SCP SoC expansion memory
0x0_3FFF_F000	0x0_3FFF_FFFF	4KB	SCC registers
0x0_4000_0000	0x0_43FF_FFFF	64MB	SCP SoC expansion
0x0_4400_0000	0x0_45FF_FFFF	32MB	SCP peripherals

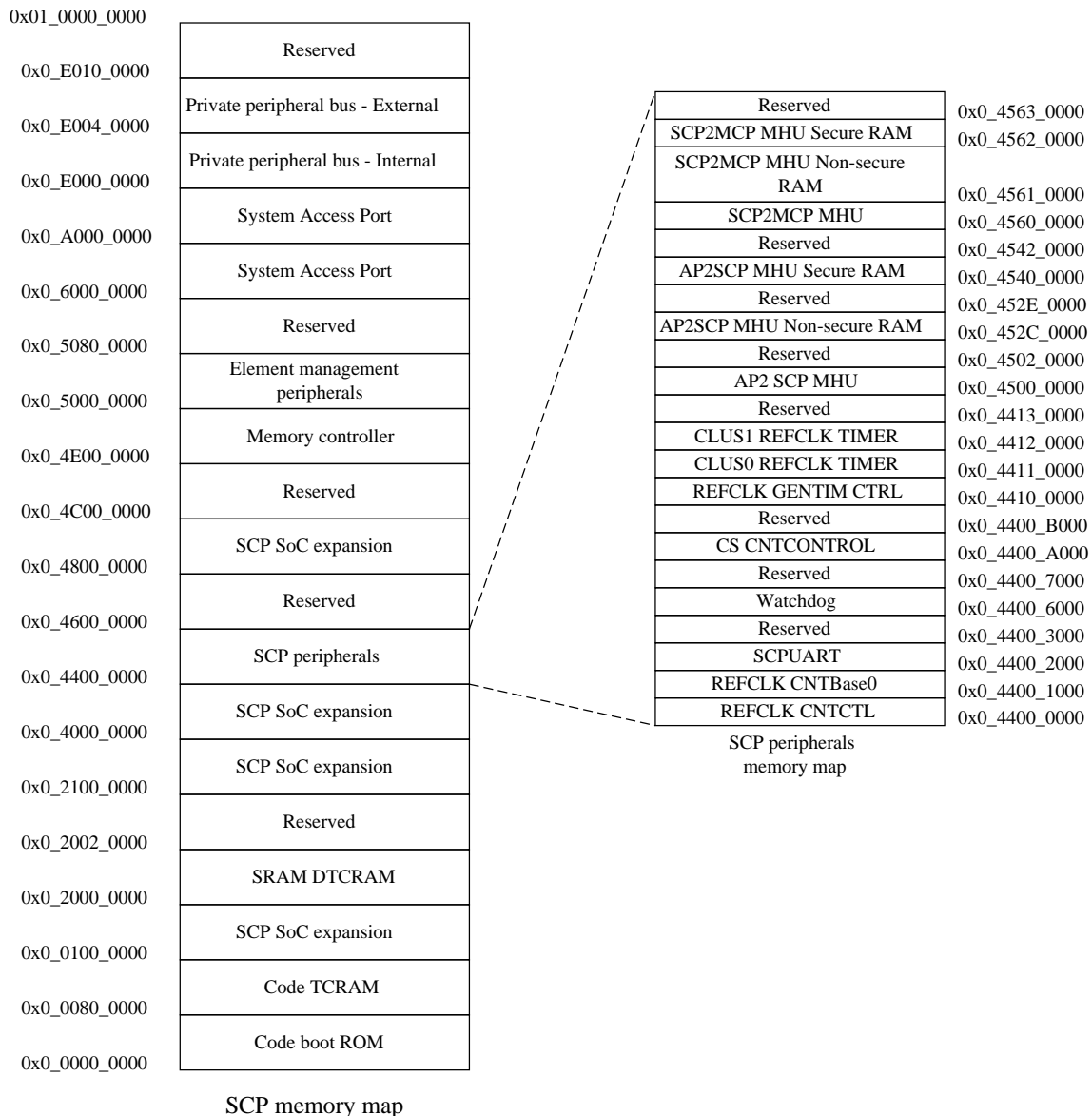
Address range from	Address range to	Size	Description
0x0_4600_0000	0x0_47FF_FFFF	32MB	Reserved
0x0_4800_0000	0x0_4BFF_FFFF	64MB	MCP SoC expansion
0x0_4C00_0000	0x0_4DFF_FFFF	32MB	Reserved
0x0_4E00_0000	0x0_4E00_FFFF	64KB	Memory element 0 configuration
0x0_4E01_0000	0x0_4E01_FFFF	64KB	Memory element 0 manager
0x0_4E02_0000	0x0_4E02_FFFF	64KB	Memory element 0 sensor group
0x0_4E03_0000	0x0_4E0F_FFFF	832KB	Reserved
0x0_4E10_0000	0x0_4E10_FFFF	64KB	Memory element 1 configuration
0x0_4E11_0000	0x0_4E11_FFFF	64KB	Memory element 1 manager
0x0_4E12_0000	0x0_4E12_FFFF	64KB	Memory element 1 sensor group
0x0_4E21_0000	0x0_4E21_FFFF	30.8125 MB	Reserved
0x0_5000_0000	0x0_507F_FFFF	8MB	Element management peripherals
0x0_5080_0000	0x0_5FFF_FFFF	248MB	Reserved
0x0_6000_0000	0x0_9FFF_FFFF	1GB	System Access Port. Translated to 0x0_4000_0000 to 0x0_7FFF_FFFF of AP memory map.
0x0_A000_0000	0x0_DFFF_FFFF	1GB	System Access Port. Translated to 0x0_0000_0000 to 0x0_3FFF_FFFF of AP memory map with debug address translation not enabled. Translated to 0x4_0000_0000 to 0x4_3FFF_FFFF of AP memory map with debug address translation enabled.
0x0_E000_0000	0x0_E003_FFFF	256KB	Private peripheral bus - Internal.
0x0_E004_0000	0x0_E00F_FFFF	768KB	Private peripheral bus - External.
0x0_E010_0000	0x0_FFFF_FFFF	511MB	Reserved

4.2.6 System Control Processor peripherals memory map

The System Control Processor (SCP) memory map of the Morello SDP contains a region associated with the SCP peripherals.

The following figure shows the peripherals region of the SCP memory map.

Figure 7: SCP peripherals memory map



The following table shows the peripherals region of the Morello SDP SCP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 8: SCP peripherals memory map

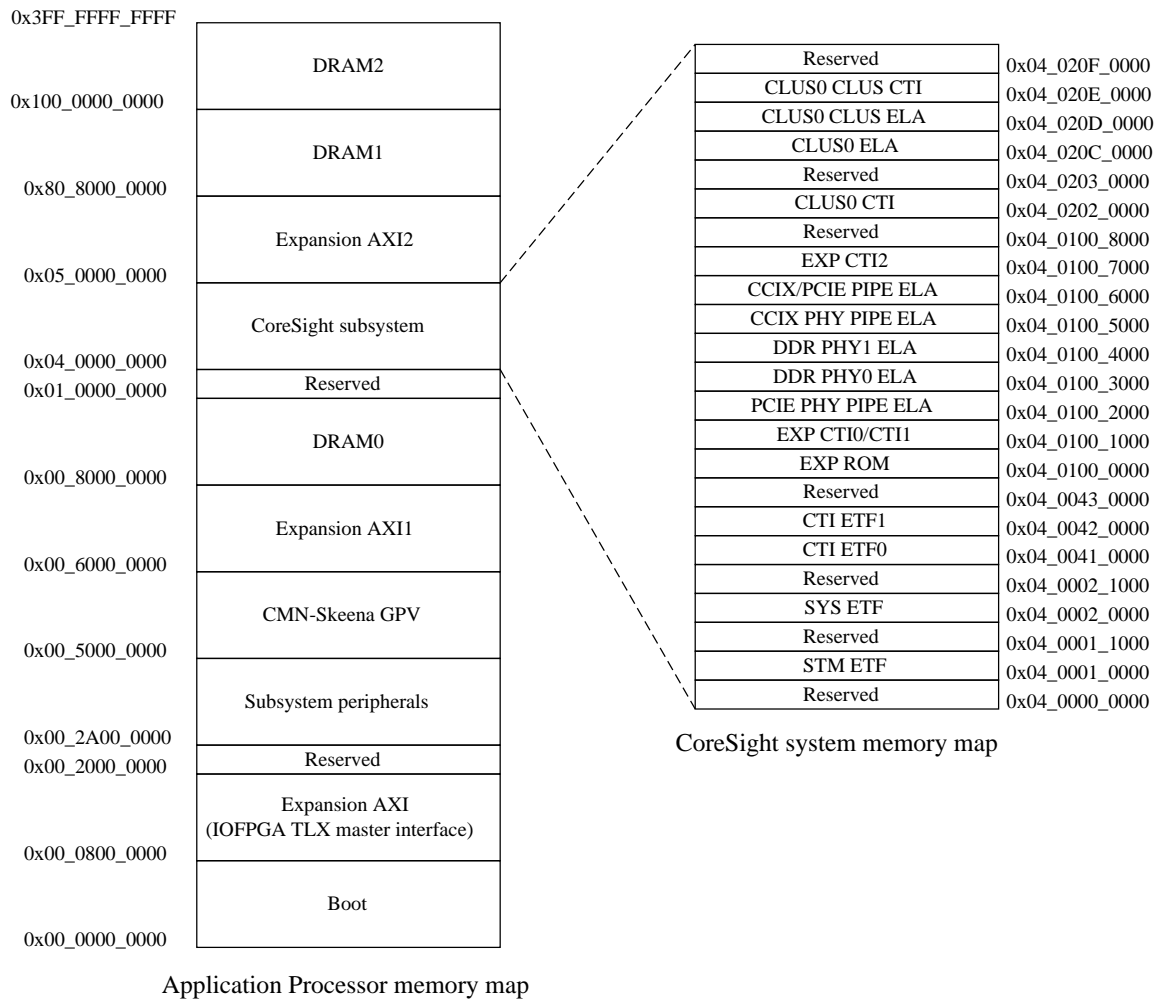
Address range from	Address range to	Size	Description
0x00_4400_0000	0x00_4400_0FFF	4KB	REFCLK CNTCTL
0x00_4400_1000	0x00_4400_1FFF	4KB	REFCLK CNTBase0
0x00_4400_2000	0x00_4400_2FFF	4KB	SCPUART
0x00_4400_6000	0x00_4400_6FFF	4KB	Watchdog (SP805)
0x00_4400_A000	0x00_4400_AFFF	4KB	CS CNTCONTROL
0x00_4410_0000	0x00_4C10_FFFF	64KB	REFCLK general timer control
0x00_4411_0000	0x00_4C41_FFFF	64KB	Cluster 0 time frame
0x00_4412_0000	0x00_4C12_FFFF	64KB	Cluster 1 time frame
0x00_4500_0000	0x00_4501_FFFF	128KB	AP2SCP Message Handling Unit (MHU)
0x00_452C_0000	0x00_452D_FFFF	128KB	AP2SCP MHU Non-secure RAM
0x00_4540_0000	0x00_4541_FFFF	128KB	AP2SCP MHU Secure RAM
0x00_4560_0000	0x00_4560_FFFF	64KB	SCP2MCH MHU
0x00_4561_0000	0x00_4561_FFFF	64KB	SCP2MCP MHU Non-secure RAM
0x00_4562_0000	0x00_4562_FFFF	64KB	SCP2MCP MHU Secure RAM
0x00_4563_0000	0x00_45FF_FFFF	64KB	Reserved

4.2.7 CoreSight system memory map

The Morello SDP Application Processor (AP) memory map contains a region that is associated with the CoreSight™ debug and trace.

The following figure shows the CoreSight™ debug and trace memory map.

Figure 8: CoreSight system memory map



The following table shows the peripherals region of the Morello SDP CoreSight™ debug and trace memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

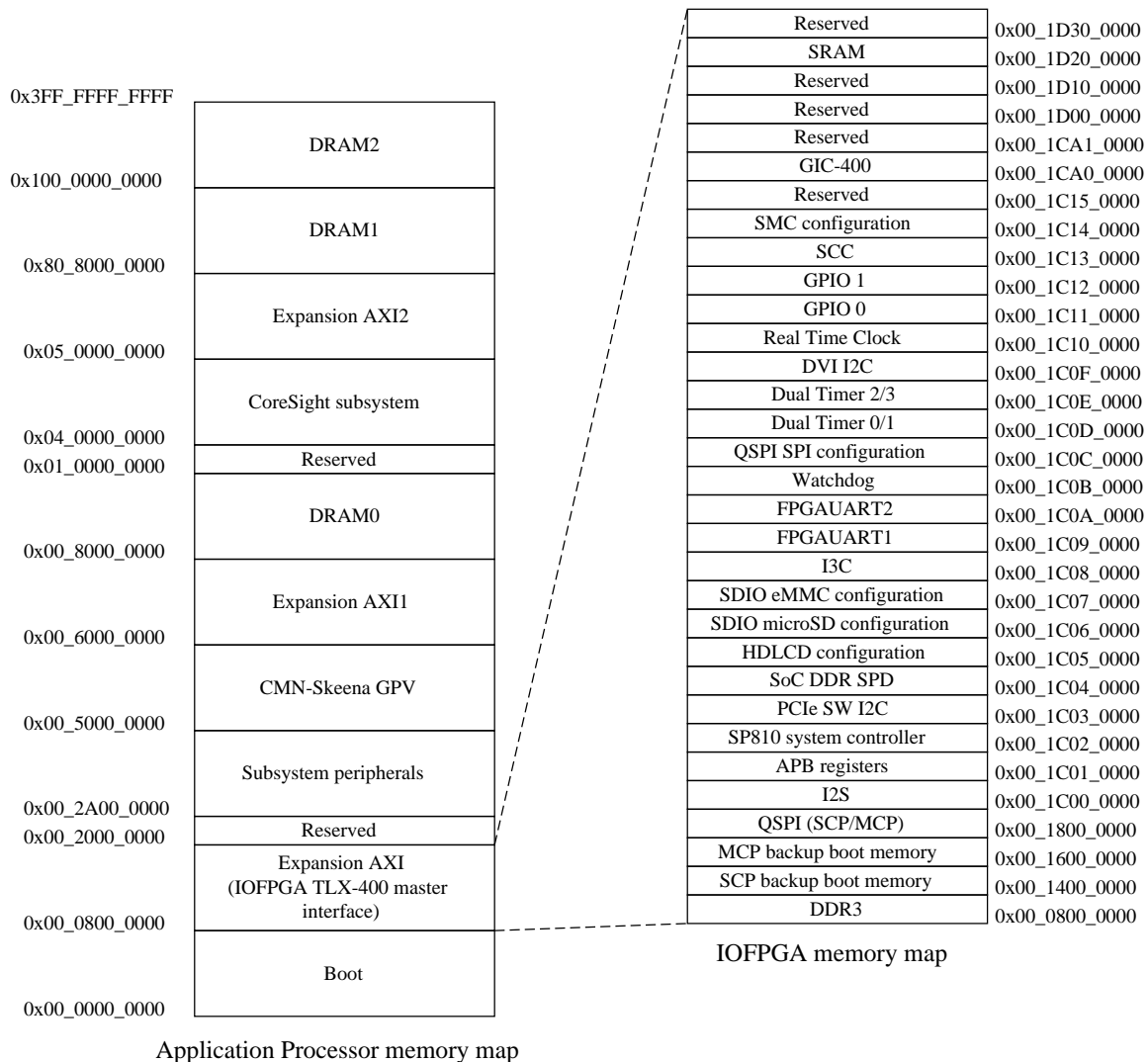
Address range From	Address range To	Size	Description
0x04_0000_0000	0x04_0000_FFFF	64KB	Reserved
0x04_0001_0000	0x04_0001_0FFF	4KB	STM ETF
0x04_0002_0000	0x04_0002_0FFF	4KB	SYS ETF
0x04_0041_0000	0x04_0041_FFFF	64KB	CTI ETF0

Address range From	Address range To	Size	Description
0x04_0042_0000	0x04_0042_FFFF	64KB	CTI ETF1
0x04_0100_0000	0x04_0100_0FFF	4KB	EXP ROM
0x04_0100_1000	0x04_0100_1FFF	4KB	EXP CTIO/CTI1
0x04_0100_2000	0x04_0100_2FFF	4KB	PCIE PHY PIPE ELA
0x04_0100_3000	0x04_0100_3FFF	4KB	DDR PHY0 ELA
0x04_0100_4000	0x04_0100_4FFF	4KB	DDR PHY1 ELA
0x04_0100_5000	0x04_0100_5FFF	4KB	CCIX PHY PIPE ELA
0x04_0100_6000	0x04_0100_6FFF	4KB	CCIX/PCIE PIPE ELA
0x04_0100_7000	0x04_0100_7FFF	4KB	EXP CTI2
0x04_0202_0000	0x04_0202_FFFF	64KB	CLUS0 CTI
0x04_020C_0000	0x04_020C_FFFF	64KB	CLUS0 ELA
0x04_020D_0000	0x04_020D_FFFF	64KB	CLUS0 CLUS ELA
0x04_020E_0000	0x04_020E_FFFF	64KB	CLUS0 CLUS CTI

4.2.8 IOFPGA memory map

The following figure shows the memory map of the peripherals inside the IOFPGA.

Figure 9: IOFPGA memory map



The following table shows the IOFPGA memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 9: IOFPGA memory map

Address range From	Address range To	Size	Description
0x0800_0000	0x13FF_FFFF	192MB	DDR3

Address range From	Address range To	Size	Description
0x1400_0000	0x15FF_FFFF	32MB	SCP backup boot memory
0x1600_0000	0x17FF_FFFF	32MB	MCP backup boot memory
0x1800_0000	0x1BFF_FFFF	32MB	QSPI (SCP/MCP)
0x1C00_0000	0x1C00_FFFF	64MB	I2S
0x1C01_0000	0x1C01_FFFF	64KB	System registers
0x1C02_0000	0x1C02_FFFF	64KB	System control
0x1C03_0000	0x1C03_FFFF	64KB	PCIe SW I2C
0x1C04_0000	0x1C04_FFFF	64KB	SoC DDR SPD
0x1C05_0000	0x1C05_FFFF	64KB	HDLCD configuration
0x1C06_0000	0x1C06_FFFF	64KB	SDIO microSD configuration
0x1C07_0000	0x1C07_FFFF	64KB	SDIO eMMC configuration
0x1C08_0000	0x1C08_FFFF	64KB	I3C
0x1C09_0000	0x1C09_FFFF	64KB	FPGAUART1
0x1C0A_0000	0x1C0A_FFFF	64KB	FPGAUART2
0x1C0B_0000	0x1C0B_FFFF	64KB	Watchdog
0x1C0C_0000	0x1C0C_FFFF	64KB	QSPI SPI configuration
0x1C0D_0000	0x1C0D_FFFF	64KB	Dual Timer 0/1
0x1C0E_0000	0x1C0E_FFFF	64KB	Dual Timer 2/3
0x1C0F_0000	0x1C0F_FFFF	64KB	DVI I2C
0x1C10_0000	0x1C10_FFFF	64KB	Real Time Clock
0x1C11_0000	0x1C11_FFFF	64KB	GPIO 0
0x1C12_0000	0x1C12_FFFF	64KB	GPIO 1

Address range From	Address range To	Size	Description
0x1C13_0000	0x1C13_FFFF	64KB	SCC
0x1C14_0000	0x1C14_FFFF	64KB	SMC configuration
0x1C15_0000	0x1C9F_FFFF	8MB	Reserved
0x1CA0_0000	0x1CA0_FFFF	64KB	GIC-400
0x1CA1_0000	0x1D1F_FFFF	8MB	Reserved
0x1D20_0000	0x1D2F_FFFF	1MB	SRAM
0x1D30_0000	0x1FFF_FFFF	45MB	Reserved

4.3 Morello SoC interrupt maps

The Morello SoC contains three independent interrupt maps for the Application Processors (APs), the System Control Processor (SCP), and the Manageability Control Processor (MCP).

GIC-600 implements two types of interrupts. Private Peripheral Interrupts (PPIs) exist separately for each core. Shared Peripheral Interrupts (SPIs) are shared between all cores. The System Control Processor (SCP) and the Manageability Control Processor (MCP) receive interrupts from several sources.

4.3.1 Application Processor interrupt map

GIC-600 implements two types of interrupts. Private Peripheral Interrupts (PPIs) exist separately for each core. Shared Peripheral Interrupts (SPIs) are shared between all cores.

The following table shows the Private Peripheral Interrupts (PPI) for the application processors. The map repeats for each core in the subsystem.

Table 10: Private peripheral interrupts

ID	Source	Description
20-16	-	Reserved
21	PMBIRQn	SPE interrupt request

ID	Source	Description
22	COMMIRQn	Debug Communications Channel receive or transmit request
23	PMUIRQn	PMU interrupt
24	CTIIRQ	CTI Interrupt
25	VCPUMNTIRQn	Virtual Maintenance Interrupt (PPI6)
26	CNTHPIRQn	Non-secure PL2 Timer event (PPI5)
27	CNTVIRQn	Virtual Timer event (PPI4)
28	CNTHVIRQn	-
29	CNTPSIRQn	Secure PL1 Physical Timer event (PPI1)
30	CNTPNSIRQn	Non-secure PL1 Physical Timer event (PPI2)
31	-	Reserved

The following table shows the Shared Peripheral Interrupts (SPI) for the application processors.

Table 11: Shared peripheral interrupts

ID	Source	Description
32	DMC0_pmuiirq	PMU event interrupt from DMC0
33	DMC0_comb_err_oflow	Combined Error interrupt overflow from DMC0
34	DMC0_failed_access_int	TZ access error interrupt from DMC0
35	DMC0_ecc_err	ECC Error from DMC0
36	DMC1_pmuiirq	PMU event interrupt from DMC1
37	DMC1_comb_err_oflow	Combined Error interrupt overflow from DMC1
38	DMC1_failed_access_int	TZ access error interrupt from DMC1
39	DMC1_ecc_err	ECC Error from DMC1
66-40	-	Reserved

ID	Source	Description
67	MCP2APMHU_NS	MHU Non-secure interrupt
68	-	Reserved
69	MCP2APMHU_S	MHU secure interrupt
70	-	Reserved
71	ETR	ETRBUFINT interrupt
72	TCU0_PRI_Q_IRPT_NS	PRI Interrupt from PCIe TCU
73	TCU1_PRI_Q_IRPT_NS	PRI interrupt from CCIX TCU
77-74	-	Reserved
78	CMN600_INTREQPMU_DTC0	PMU Count Overflow Interrupt
82-79	-	Reserved
83	STM-500	STM-500 Synchronization Interrupt
84	CTI	CTI Trigger output 6 from CTI2
85	CTI	CTI Trigger output 7 from CTI2
86	Trusted Watchdog	Trusted Watchdog interrupt(WSO)
87	AP_SEC_UART_INT	AP secure UART interrupt.
90-88	-	Reserved
91	AP_REFCLK Generic Timer (Secure)	AP_REFCLK Generic Timer Interrupt (Secure)
92	AP_REFCLK Generic Timer (Non-secure)	AP_REFCLK Generic Timer Interrupt (Non-secure)
93	Generic Watchdog	Watchdog WSO Interrupt
94	Generic Watchdog	Watchdog WS1 Interrupt
95	AP0 UART	AP UART0 interrupt
96	AP2 UART	AP UART2 interrupt

ID	Source	Description
97	GPU	GPU interrupt request
98	GPU	Job interrupt request
99	GPU	MMU interrupt request
100	GPU	GPU event request (Reserved for Odin/Griff)
101	Display	Interrupt output from Global Control Unit of the DPU
102	Display	Interrupt output from AFBC DMA Unit of the DPU
103	-	Reserved
104	DISPLAY0 TBU	TBU PMU IRPT
105	-	Reserved
106	-	Reserved
107	DISPLAY TCU	Event Queue Secure interrupt, indicating Event Queue Non-Empty or Overflow event_q_irpt_s
108	DISPLAY TCU	Event Queue Non-Secure interrupt, indicating Event Queue Non-Empty or Overflow event_q_irpt_ns
109	DISPLAY TCU	Reserved
110	DISPLAY TCU	SYNC Complete Non-secure Interrupt cmd_sync_irpt_ns
111	DISPLAY TCU	SYNC Complete Secure interrupt cmd_sync_irpt_s
112	DISPLAY TCU	Global Non-secure interrupt global_irpt_ns
113	DISPLAY TCU	Global Secure interrupt global_irpt_s
114	-	Reserved
115	DISPLAY TCU	pmu_irpt PMU (Performance Monitor Unit) interrupt
125-116	-	Reserved
126	CLUS0_PMUIRQn	DSU PMU interrupt

ID	Source	Description
127	CLUSO_PMUIRQn	DSU PMU interrupt
128	Morello board	AP external IRQ (AP_EXT_INT)
129	Morello board	AP external Ethernet IRQ (AP_EXT_ETHERNET_INT)
167-130	-	Reserved
168	Morello SoC	GPIO IOFPGA combined IRQ
176-169	Morello SoC	GPIO IOFPGA combined IRQ [7:0]
200-177	-	Reserved
201	Morello SoC	pcie_inta_out
202	Morello SoC	pcie_intb_out
203	Morello SoC	pcie_intc_out
204	Morello SoC	pcie_intd_out
205	Morello SoC	pcie_phy_interrupt_out
206	Morello SoC	pcie_aer_interrupt
207	Morello SoC	pcie_link_down_reset_out
208	Morello SoC	pcie_local_interrupt_reset
209	Morello SoC	pcie_performance_data_threshold
210	Morello SoC	pcie_negotiated_speed_change
211	Morello SoC	pcie_link_training_done
212	Morello SoC	pcie_pll_status_rise
213	Morello SoC	pcie_message_fifo_interrupt
214	Morello SoC	pcie_local_interrupt_ras
215	Morello SoC	pcie_phy_lane_interrupt

ID	Source	Description
231-216	-	Reserved
232	Morello SoC	ccix_bus_device_change_irq
233	Morello SoC	ccix_inta_out
234	Morello SoC	ccix_intb_out
235	Morello SoC	ccix_intc_out
236	Morello SoC	ccix_intd_out
237	Morello SoC	ccix_phy_interrupt_out
238	Morello SoC	ccix_aer_interrupt
239	Morello SoC	ccix_link_down_reset_out
240	Morello SoC	ccix_local_interrupt_reset
241	Morello SoC	ccix_performance_data_threshold
242	Morello SoC	ccix_negotiated_speed_change
243	Morello SoC	ccix_link_training_done
244	Morello SoC	ccix_pll_status_rise
245	Morello SoC	ccix_message_fifo_interrupt
246	Morello SoC	ccix_local_interrupt_ras
247	Morello SoC	ccix_hot_reset_irq
248	Morello SoC	ccix_flr_reset_irq
249	Morello SoC	ccix_power_state_change_irq
250	Morello SoC	ccix_phy_lane_interrupt
255-251	-	Reserved
256	MMUTCU1_PMU_IRPT	PMU interrupt

ID	Source	Description
257	MMUTCU1_EVENT_Q_IRPT_S	Event Queue Secure interrupt, indicating Event Queue Non-Empty or Overflow
258	MMUTCU1_CMD_SYNC_IRPT_S(SYNC Complete Secure interrupt
259	MMUTCU1_GLOBAL_IRPT_S	Global Secure interrupt
260	MMUTCU1_EVENT_Q_IRPT_NS	Event Queue non-Secure interrupt, indicating Event Queue Non-Empty or Overflow
261	MMUTCU1_CMD_SYNC_IRPT_NS	SYNC Complete Non-secure interrupt
262	MMUTCU1_GLOBAL_IRPT_NS	Global Non-secure interrupt
263	MMUTCU2_PMU_IRPT	PMU interrupt
264	MMUTCU2_EVENT_Q_IRPT_S	Event Queue Secure interrupt, indicating Event Queue Non-Empty or Overflow
265	MMUTCU2_CMD_SYNC_IRPT_S	SYNC Complete Secure interrupt
266	MMUTCU2_GLOBAL_IRPT_S	Global Secure interrupt
267	MMUTCU2_EVENT_Q_IRPT_NS	Event Queue non-Secure interrupt, indicating Event Queue Non-Empty or Overflow
268	MMUTCU2_CMD_SYNC_IRPT_NS	SYNC Complete Non-secure interrupt
269	MMUTCU2_GLOBAL_IRPT_NS	Global Non-secure interrupt
319-270	-	Reserved
323-320	MMUTBU_PMU_IRPT[3:0]	TBU PMU Interrupt. Allocated to 4 TBUs in the system.
511-324	-	Reserved
512	CLUSTER0SCP ->AP MHU Non-secure	-
513	CLUSTER0SCP ->AP MHU secure	-
514	CLUSTER1SCP ->AP MHU Non-secure	-
515	CLUSTER1SCP ->AP MHU secure	-

ID	Source	Description
575-516	-	Reserved
576	P0_REFCLK_GENTIM	Pn_REFCLK Generic Secure Timer interrupts
577	P0_REFCLK_GENTIM	Pn_REFCLK Generic Secure Timer interrupts
640-578	-	Reserved

4.3.2 System Control Processor interrupt map

The System Control Processor (SCP) receives interrupts from several sources.

The sources of the interrupts to the SCP are:

- Application Processor system wakeup interrupts
- CoreSight™ power and reset request interrupts
- Internal SCP subsystem interrupts
- Expansion SCP interrupts

The interrupts are routed to the Nested Vector Interrupt Controllers in Cortex®-M7 processors where they can be managed by software.

The following table shows the SCP interrupts.

Table 12: SCP interrupts

ID	Source	Description
NMI	SCP Generic Watchdog	SCP Watchdog (WS0)
0	-	Reserved
1	CoreSight	CoreSight debug power up request (If there is a separate debug power domain). Note: SCP Firmware must support optional debug power up rail.
2	CoreSight	CoreSight system power up request
3	CoreSight	CoreSight debug reset request
4	GIC expansion interrupt	External GIC wakeup interrupt. Generated by the logical OR of all the GIC Expansion Interrupts.

ID	Source	Description
15-5	-	Reserved
16	SCP external IRQ (SCP_EXT_INT)	SCP external IRQ (SCP_EXT_INT)
17	GPIO pads	GPIO-IOFPGA combined IRQ
25-18	GPIO pads	GPIO-IOFPGA individual IRQ[7:0] and IOFPGA external IRQ[7:0]
32-26	-	Reserved
33	SCP REFCLK Generic Timer	REFCLK Physical Timer interrupt
34	GENTIM_SYNC	System generic timer synchronization interrupt
35	CSTS_SYNC	CoreSight Time stamp synchronization interrupt
36	-	Reserved
37	CTI	CTI Trigger 0
38	CTI	CTI Trigger 1
39	GICECCFATAL	GIC Fatal ECC failure
40	GICAXIMERR	GIC Fatal AXI Master error
41	-	Reserved
42	AON_UART_INT	Always-on UART interrupt
43	-	Reserved
44	Generic Watchdog	Generic Watchdog timer interrupt WS0
45	Generic Watchdog	Generic Watchdog timer interrupt WS1
46	Trusted Watchdog	Trusted Watchdog timer interrupt WS0
47	Trusted Watchdog	Trusted Watchdog timer interrupt WS1
48	APPS_UART_INT	Applications UART interrupt
49	-	Reserved

ID	Source	Description
50	CPU Core Power Policy Units	Consolidated CPU PPU Interrupt for cores
53-51	-	Reserved
54	CPU Cluster Power Policy Units	Consolidated CPU cluster PPU Interrupt for clusters 0-1
55	CPU Core PLLs	Consolidated CPU PLL Lock for PLLs
58-56	-	Reserved
59	CPU Core Fault Indicator	Consolidated nFaultIRQ for both clusters
63-60	-	Reserved
64	CPU ECC error interrupts	Consolidated nERRIRQ for both clusters
68-64	-	Reserved
69	Cluster PLLs	Consolidated lock interrupt for cluster PLLs
70	Cluster PLLs	Consolidated unlock interrupt for cluster PLLs
71	dso_clu0_irq0	Cluster0 DSO interrupt0
72	dso_clu0_irq1	Cluster0 DSO interrupt1
73	dso_clu1_irq0	Cluster1 DSO interrupt0
74	dso_clu1_irq1	Cluster1 DSO interrupt1
81-75	-	Reserved
82	AP2SCP MHU Non-secure interrupt	Consolidated MHU High Priority Non-Secure interrupt
83	AP2SCP MHU Secure interrupt	Consolidated MHU Secure interrupt for both clusters
84	MCP2SCP MHU Non-secure Interrupt	MCP2SCP MHU High Priority Interrupt
85	MCP2SCP MHU Secure Interrupt	MCP2SCP MHU High Priority Interrupt
89-86	-	Reserved

ID	Source	Description
90	Pn_REFCLK _GENTIM_1_2	Consolidated Pn REFCLK Timer Interrupt for both clusters
93-91	-	Reserved
94	CONS _MMU_TCU_RASIRPT	Consolidated MMU RAS for the interrupt coming from multiple TCUs
95	CONS_MMU_TBU_RAS IRPT[NUM_TBUS-1:0]	Consolidated TBU for the interrupts coming from various TBUs
96	INTREQPPU	PPU interrupt from CMN-Ske
97	INTREQERRNS	Non Secure error handling interrupt from CMN-Skeena
98	INTREQERRS	Secure error handling interrupt from CMN-Skeena
99	INTREQFAULTS	Secure Fault handling interrupt from CMN-Skeena
100	INTREQFAULTNS	Non Secure Fault handling interrupt from CMN-Skeena
101	INTREQPMU	PMU count overflow interrupt
119-102	-	Reserved
127-120	DBGCH [0-7]_PPU_INT	-
129	-	Reserved
130	Power Integration Kit	Debug PIK Interrupt
131	LOGIC_PPU_INT	LOGIC_PPU_INT
134-132	-	Reserved
135	SRAM_PPU_INT	SRAM PPU Interrupt
136	DPU_PPU_INT	Display PPU Interrupt
137	GPU_PPU_INT	GPU PPU Interrupt
138	-	Reserved

ID	Source	Description
139	MCP WS1	MCP Watchdog reset
140	SYSPLL_LOCK	Sys PLL Lock
141	SYSPLL_UNLOCK	Sys PLL Unlock
142	INTPLL_LOCK	Interconnect PLL Lock
143	INTPLL_UNLOCK	Interconnect PLL UnLock
144	DPUPLL_LOCK	DISPLAY PLL Lock
145	DPUPLL_UNLOCK	DISPLAY PLL UnLock
146	GPUPLL_LOCK	GPU PLL Lock
147	GPUPLL_UNLOCK	GPU PLL UnLock
148	PXLPLL_LOCK	Pixel PLL Lock
149	PXLPLL_UNLOCK	Pixel PLL Unlock
173-150	-	Reserved
174	DMC_PLL_LOCK	DMC PLL Lock
175	DMC_PLL_UNLOCK	DMC PLL Unlock
179-176	-	Reserved
180	DMC0 Interrupt	DMC0_misc oflow
181	DMC0 Interrupt	DMC0_err_oflow
182	DMC0 Interrupt	DMC0_ecc_err_int
183	DMC0 Interrupt	DMC0_misc_access_int
184	DMC0 Interrupt	DMC0_temperature_event_int
185	DMC0 Interrupt	DMC0_failed_access_int
186	DMC0 Interrupt	DMC0_mgr_int

ID	Source	Description
187	DMC1 Interrupt	DMC1_misc oflow
188	DMC1 Interrupt	DMC1_err_oflow
189	DMC1 Interrupt	DMC1_ecc_err_int
190	DMC1 Interrupt	DMC1 _misc_access_int
191	DMC1 Interrupt	DMC1 _te mperature_event_int
192	DMC1 Interrupt	DMC1 _failed_access_int
193	DMC1 Interrupt	DMC1_mgr_int
208	SCP C2C I2C	SCP C2C I2C interrupt (I2C0)
209	SCP PMIC I2C	SCP PMIC I2C interrupt (I2C1)
210	SCP SPD-PCC I2C	SCP SPD-PCC I2C interrupt (I2C2)
211	SCP-QSPI	SCP QSPI interrupt
212	PVT controller	PVT controller interrupt
218-213	-	Reserved
219	ccix_bus _device_change_irq	ccix_bus _device_change_irq
220	ccix_inta_out	ccix_inta_out
221	ccix_intb_out	ccix_intb_out
222	ccix_intc_out	ccix_intc_out
223	ccix_intd_out	ccix_intd_out
224	ccix_phy_interrupt_out	ccix_phy_interrupt_out
225	ccix_aer_interrupt	ccix_aer_interrupt
226	ccix_l ink_down_reset_out	ccix_l ink_down_reset_out
227	ccix_lo cal_interrupt_reset	ccix_lo cal_interrupt_reset

ID	Source	Description
228	ccix_perform ance_data_threshold	ccix_perform ance_data_threshold
229	ccix_nego tiated_speed_change	ccix_nego tiated_speed_change
230	ccix_ link_training_done	ccix_ link_training_done
231	cc ix_pll_status_rise	cc ix_pll_status_rise
232	ccix_mes sage_fifo_interrupt	ccix_mes sage_fifo_interrupt
233	ccix_ local_interrupt_ras	ccix_ local_interrupt_ras
234	ccix_hot_reset_irq	ccix_hot_reset_irq
235	ccix_flr_reset_irq	ccix_flr_reset_irq
236	ccix_powe r_state_change_irq	ccix_powe r_state_change_irq
237	pcie_aer_interrupt	pcie_aer_interrupt
238	pcie_lo cal_interrupt_reset	pcie_lo cal_interrupt_reset
239	pcie_ local_interrupt_ras	pcie_ local_interrupt_ras

4.3.3 Manageability Control Processor interrupt map

The Manageability Control Processor (MCP) receives interrupts from several sources.

The sources of the interrupts to the MCP are:

- Application Processor system wakeup interrupts
- CoreSight™ power and reset request interrupts
- Internal MCP subsystem interrupts
- Expansion MCP interrupts

The interrupts are routed to the Nested Vector Interrupt Controllers in Cortex®-M7 processors where they can be managed by software.

The following table shows the MCP interrupts.

Table 13: MCP interrupts

ID	Source	Description
NMI	MCP Generic Watchdog	MCP Watchdog (WS0)
0	-	Reserved
1	CoreSight	CoreSight debug power up request (If there is a separate debug power domain). Note: MCP Firmware must support optional debug power up rail.
2	CoreSight	CoreSight system power up request
3	CoreSight	CoreSight debug reset request
4	GIC expansion interrupt	External GIC wakeup interrupt. Generated by the logical OR of all the GIC Expansion Interrupts.
15-5	-	Reserved
16	MCP external IRQ (MCP_EXT_INT)	MCP external IRQ (MCP_EXT_INT)
17	GPIO pads	GPIO-IOFPGA combined IRQ
25-18	GPIO pads	GPIO-IOFPGA individual IRQ[7:0] and IOFPGA external IRQ[7:0]
32-26	-	Reserved
33	MCP REFCLK Generic Timer	REFCLK Physical Timer interrupt
34	Non-secure AP2MCP MHU	MHU Non-Secure interrupt
35	-	Reserved
36	AP2MCP Secure MHU	MHU Secure interrupt
37	CTI	CTI Trigger 0
38	CTI	CTI Trigger 1
41-39	-	Reserved
42	MCP_UART0_INT	Always-on UART interrupt
83-43	MCP_UART1_INT	Always-on UART interrupt

ID	Source	Description
84	MCP2SCP MHU Non-secure Interrupt	MCP2SCP MHU High Priority Interrupt
85	MCP2SCP MHU Secure Interrupt	MCP2SCP MHU High Priority Interrupt
93-86	-	Reserved
94	MMU_TBU_RASIRPT[NUM_TBUS-1:0]	Consolidated MMU RAS for the interrupt coming from multiple TCUs
95	MMU_TBU_RASIRPT[NUM_TBUS-1:0]	Consolidated TBU for the interrupts coming from multiple TBUs
96	INTREQPPU	PPU interrupt from CMN-Skeena
97	INTREQERRNS	Non-secure error handling interrupt from CMN-Skeena
98	INTREQERRS	Secure error handling interrupt from CMN-Skeena
99	INTREQFAULTS	Secure Fault handling interrupt from CMN-Skeena
100	INTREQFAULTNS	Non-secure Fault handling interrupt from CMN-Skeena
101	INTREQPMU	PMU count overflow interrupt
138-102	-	Reserved
139	MCP WS1	MCP Watchdog reset
179-140	SYSPLL_LOCK	Sys PLL Lock
180	DMCO Interrupt	DMCO_misc oflow
181	DMCO Interrupt	DMCO_err_oflow
182	DMCO Interrupt	DMCO_ecc_err_int
183	DMCO Interrupt	DMCO_misc_access_int
184	DMCO Interrupt	DMCO_temperature_event_int
185	DMCO Interrupt	DMCO_failed_access_int
186	DMCO Interrupt	DMCO_mgr_int

ID	Source	Description
187	DMC1 Interrupt	DMC1_misc oflow
188	DMC1 Interrupt	DMC1_err_oflow
189	DMC1 Interrupt	DMC1_ecc_err_int
190	DMC1 Interrupt	DMC1_misc_access_int
191	DMC1 Interrupt	DMC1_temperature_event_int
192	DMC1 Interrupt	DMC1_failed_access_int
193	DMC1 Interrupt	DMC1_mgr_int
208	MCP C2C I2C	MCP C2C I2C interrupt (I2C0)
209	MCP BMC-PCC I2C	MCP BMC-PCC I2C interrupt (I2C1)
210	MCP-QSPI	MCP QSPI interrupt
219-211	-	Reserved
220	pcie_aer_interrupt	pcie_aer_interrupt
221	pcie_local_interrupt_reset	pcie_local_interrupt_reset
222	pcie_local_interrupt_ras	pcie_local_interrupt_ras
223	ccix_aer_interrupt	ccix_aer_interrupt
224	ccix_local_interrupt_reset	ccix_phy_interrupt_out
225	ccix_local_interrupt_ras	ccix_aer_interrupt
239-226	ccix_link_down_reset_out	ccix_link_down_reset_out

4.4 System Security Control registers

The System Security Control (SSC) interface in the Morello SoC controls system-wide security features.

These features include the following:

- Selection of an internal sources for Debug Authentication signals
- General Purpose register for secure state storage

4.4.1 System Security Control registers summary

The base memory address of the SSC registers is 0x0_2A42_0000 in the subsystem peripherals region of the Application Processor (AP) memory map.

The following table shows the SSC registers in offset order from the base memory address. Undefined registers are reserved. Software must not attempt to access these registers.

Base memory address
0x0_2A42_0000

Table 14: SSC registers summary

Offset	Name	Type	Reset	Width	Description
0x0010	SSC_DBG_CFG_STAT	RO	0x0001_0000	32	See SSC_DBGCFG_STAT Register .
0x0014	SSC_DBGCFG_SET	WO	N/A	32	See SSC_DBGCFG_SET Register .
0x0018	SSC_DBGCFG_CLR	WO	N/A	32	See SSC_DBGCFG_CLR Register .
0x0028	SSC_AUXDBGCFG	RW	0x0000_0000	32	See SSC_AUXDBGCFG Register .
0x0030	SSC_GPRETN	RW	0x0000_0000	32	See SSC_GPRETN Register .
0x0040	SSC_VERSION	RO	0x1004_17B3	32	See SSC_VERSION Register .
0x0500	SSC_CHIPID_ST	RO	0x0000_0000	32	See SSC_CHIPID_ST Register .
0x0FD0	SSC_PID4	RO	0x0000_0004	32	See SSC_PID4 Register .
0x0FE0	SSC_PID0	RO	0x0000_0044	32	See SSC_PID0 Register .
0x0FE4	SSC_PID1	RO	0x0000_00B8	32	See SSC_PID1 Register .
0x0FE8	SSC_PID2	RO	0x0000_000B	32	See SSC_PID2 Register .
0x0FF0	COMPID0	RO	0x0000_000D	32	See SSC_COMPID0 Register .

Offset	Name	Type	Reset	Width	Description
0x0FF4	COMPID1	RO	0x0000_00F0	32	See SSC_COMPID1 Register .
0x0FF8	COMPID2	RO	0x0000_0005	32	See SSC_COMPID2 Register .
0x0FFC	COMPID3	RO	0x0000_00B1	32	See SSC_COMPID3 Register .

4.4.2 SSC_DBGCFG_STAT Register

The SSC_DBGCFG_STAT Register characteristics are:

Purpose

Controls how the Debug Authentication signals are to be driven, either from an external source, or internally using build-in register bits, also implemented using this register.

Defines the values of the Debug Authentication signals when they are configured to be internally driven.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_DBGCFG_STAT Register bit assignments.

Table 15: SSC_DBGCFG_STAT Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7]	SPIDEN_SEL_STAT	RO	<p>Selects between SPIDEN external or internal drive:</p> <p>0b0: External.</p> <p>0b1: Internal.</p> <p>If external mode is selected SPIDEN is driven by top-level configuration input SPIDEN_CFG.</p> <p>Reset value 0b0.</p>

Bits	Name	Type	Function
[6]	SPIDEN_INT_STAT	RO	SPIDEN internal drive value. Reset value 0b0.
[5]	SPNIDEN_SEL_STAT	RO	Selects between SPNIDEN external or internal drive: 0b0: External. 0b1: Internal. If external mode is selected SPNIDEN is driven by top-level configuration input. Reset value 0b0.
[4]	SPNIDEN_INT_STAT	RO	SPNIDEN internal drive value. Reset value 0b0.
[3]	DEVICEEN_SEL_STAT	RO	Selects between DEVICEEN external or internal drive: 0b0: External. 0b1: Internal. If external mode is selected DEVICEEN is driven by top-level configuration input. Reset value 0b0.
[2]	DEVICEEN_INT_STAT	RO	DEVICEEN internal drive value. Reset value 0b0.
[1:0]	-	-	Reserved.

4.4.3 SSC_DBGCFG_SET Register

The SSC_DBGCFG_SET Register characteristics are:

Purpose

The SSC_DBGCFG_SET register is a Secure access only write-only memory mapped register. This register is associated with the SSC_DBGCFG_STAT register. Writing 0b1 to a particular field in the SSC_DBGCFG_SET register sets the corresponding bit in the SSC_DBGCFG_STAT register to 1.

Usage constraints

This register is write-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_DBGCFG_SET Register bit assignments.

Table 16: SSC_DBGCFG_SET Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7]	SPIDEN_SEL_SET	RO	Sets SPIDEN_SEL_STAT to 0b1: 0b0: No effect. 0b1: Set SPIDEN_SEL_STAT to 0b1.
[6]	SPIDEN_INT_SET	RO	Sets SPIDEN_INT_STAT to 0b1: 0b0: No effect. 0b1: Set SPIDEN_INT_STAT to 0b1.
[5]	SPNIDEN_SEL_SET	RO	Sets SPNIDEN_SEL_STAT to 0b1: 0b0: No effect. 0b1: Set SPNIDEN_INT_STAT to 0b1.
[4]	SPNIDEN_INT_SET	RO	Sets SPNIDEN_INT_STAT to 0b1: 0b0: No effect. 0b1: Set SPNIDEN_INT_STAT to 0b1.
[3]	DEVI CEEN_SEL_SET	RO	Sets DEVI CEEN_SEL_STAT to 0b1: 0b0: No effect. 0b1: Set DEVI CEEN_SEL_STAT to 0b1.
[2]	DEVI CEEN_INT_SET	RO	Sets DEVI CEEN_INT_STAT to 0b1: 0b0: No effect. 0b1: Set DEVI CEEN_INT_STAT to 0b1.

Bits	Name	Type	Function
[1:0]	-	-	Reserved.

4.4.4 SSC_DBGCFG_CLR Register

The SSC_DBGCFG_CLR Register characteristics are:

Purpose

The SSC_DBGCFG_CLR register is a Secure access only write-only memory mapped register. This register is associated with the SSC_DBGCFG_STAT register. Writing 0b1 to a particular field in the SSC_DBGCFG_CLR register clears the corresponding bit in the SSC_DBGCFG_STAT register to 0.

Usage constraints

This register is write-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_DBGCFG_CLR Register bit assignments.

Table 17: SSC_DBGCFG_CLR Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7]	SPIDEN_SEL_CLR	WO	Clears SPIDEN_SEL_STAT to 0b1: 0b0: No effect. 0b1: Clear SPIDEN_SEL_STAT to 0b0.
[6]	SPIDEN_INT_CLR	WO	Clears SPIDEN_INT_STAT to 0b1: 0b0: No effect. 0b1: Clear SPIDEN_INT_STAT to 0b0.

Bits	Name	Type	Function
[5]	SPNIDEN_SEL_CLR	WO	Clears SPNIDEN_SEL_STAT to 0b1: 0b0: No effect. 0b1: Clear SPNIDEN_INT_STAT to 0b0.
[4]	SPNIDEN_INT_CLR	WO	Clears SPNIDEN_INT_STAT to 0b1: 0b0: No effect. 0b1: Clear SPNIDEN_INT_STAT to 0b0.
[3]	DEVICEEN_SEL_CLR	WO	Clears DEVICEEN_SEL_STAT to 0b1: 0b0: No effect. 0b1: Clear DEVICEEN_SEL_STAT to 0b0.
[2]	DEVICEEN_INT_CLR	WO	Clears DEVICEEN_INT_STAT to 0b0: 0b0: No effect. 0b1: Clear DEVICEEN_INT_STAT to 0b0.
[1:0]	-	-	Reserved.

4.4.5 SSC_AUXDBGCFG Register

The SSC_AUXDBGCFG Register characteristics are:

Purpose

The SSC_AUXDBGCFG register is a Secure access only read-write register. The register provides override control of the debug authentication signals **DBGEN** and **NIDEN**.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_AUXDBGCFG Register bit assignments.

Table 18: SSC_AUXDBGCFG Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1:0]	INTERNAL_DEBUG_OVERRIDE	RW	<p>0b00: Enable Non-secure self-hosted debug. DBGEN and NIDEN inputs to the application processors are HIGH.</p> <p>0b01: Disable Invasive, Non-secure self-hosted debug.</p> <p>Enable Non-invasive, Non-secure self-hosted debug.</p> <p>DBGEN inputs to the application processors are LOW and NIDEN inputs to the application processors are HIGH.</p> <p>0b1: Disable Non-secure self-hosted debug.</p> <p>DBGEN and NIDEN inputs to the application processors are LOW.</p> <p>Reset value 0b00.</p>



Arm strongly recommends that this register is not used, and that you leave both bits at their reset value.

4.4.6 SSC_GPRETN Register

The SSC_GPRETN Register characteristics are:

Purpose

The SSC_GPRETN register is a Secure access read/write memory mapped register that provides 16 bit general storage for security purposes. The register resets only on system powerup reset.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_GPRETN Register bit assignments.

Table 19: SSC_GPRETN Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:0]	GPRETN	RW	General-purpose register for Secure state storage. Reset value 0x0000.

4.4.7 SSC_VERSION Register

The SSC_VERSION Register characteristics are:

Purpose

The SSC_VERSION register is a Secure access read-only memory mapped register that specifies the Morello SoC version ID for security purposes.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_VERSION Register bit assignments.

Table 20: SSC_VERSION Register bit assignments

Bits	Name	Type	Function
[31:28]	CONFIGURATION	RO	Equals 0b0001 on Morello SoC.
[27:24]	MAJOR_REVISION	RO	Equals 0b0000 on Morello SoC.
[23:20]	MINOR_REVISION	RO	Equals 0b0000 on Morello SoC.
[19:12]	DESIGNER_ID	RO	Equals Arm identifier 0x41 on Morello SoC.
[11:0]	PART_NUMBER	RO	Equals Arm identifier 0x7B3 on Morello SoC.

4.4.8 SSC_CHIPID_ST Register

The SSC_CHIPID_ST Register characteristics are:

Purpose

The SSC_CHIPID_ST register stores the CHIPID status for the node when there are multiple sockets.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_CHIPID_ST Register bit assignments.

Table 21: SSC_CHIPID_ST Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[8]	MU_LTI_CHIP_MODE	RO	Multi-chip mode tie-off value. 0: Single chip. 1: Multi-chip. Reset value 0b0.
[7:6]	-	-	Reserved.
[5:0]	CHIP_ID	RO	Tie-off value in multi-chip mode. This is 0b0 for single chip mode. Reset value 0b000000

4.4.9 SSC_PID4 Register

The SSC_PID4 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_PID4 Register bit assignments.

Table 22: SSC_PID4 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:4]	SIZE	RO	LOG2 of the number of 4KB blocks occupied by the interface. Reset value 0x0.
[3:0]	DES_2	RO	JEP106 continuation code to identify designer. Reset value 0x4 for Arm.

4.4.10 SSC_PID0 Register

The SSC_PID0 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_PID0 Register bit assignments.

Table 23: SSC_PID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.

Bits	Name	Type	Function
[7:0]	PART_0	RO	Bits [7:0] of part number. Reset value 0x44.

4.4.11 SSC_PID1 Register

The SSC_PID1 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_PID1 Register bit assignments.

Table 24: SSC_PID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:4]	DES_0	RO	Bits[3:0] of JEP identity. Reset value 0xB.
[3:0]	PART_1	RO	Bits[11:8] of part number. Reset value 0x8.

4.4.12 SSC_PID2 Register

The SSC_PID2 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_PID2 Register bit assignments.

Table 25: SSC_PID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:4]	REVISION	RO	Revision number. Reset value 0x0.
[3]	JEDEC	RO	JEDEC ID. Reset value 0b1.
[2:0]	DES_1	RO	Designer ID. Reset value 0b011.

4.4.13 SSC_COMPID0 Register

The SSC_COMPID0 Register characteristics are:

Purpose

The SSC_COMPID0 register stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_COMPID0 Register bit assignments.

Table 26: SSC_COMPID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	SSC_COMPID0	RO	Component ID 0 information. Reset value 0x0D.

4.4.14 SSC_COMPID1 Register

The SSC_COMPID1 Register characteristics are:

Purpose

The SSC_COMPID1 register stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_COMPID1 Register bit assignments.

Table 27: SSC_COMPID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	SSC_COMPID1	RO	Component ID 1 information. Reset value 0xF0.

4.4.15 SSC_COMPID2 Register

The SSC_COMPID2 Register characteristics are:

Purpose

The SSC_COMPID2 register stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_COMPID2 Register bit assignments.

Table 28: SSC_COMPID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	SSC_COMPID2	RO	Component ID 2 information. Reset value 0x05.

4.4.16 SSC_COMPID3 Register

The SSC_COMPID3 Register characteristics are:

Purpose

The SSC_COMPID3 register stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Security Control registers summary](#).

The following table shows the SSC_COMPID3 Register bit assignments.

Table 29: SSC_COMPID3 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	SSC_COMPID3	RO	Component ID 3 information. Reset value 0xB1.

4.5 System Configuration Control registers

The System Configuration Control (SCC) registers contain the initial settings of blocks before bootup. Write and read accesses to these registers during run-time enable software to alter and to read block settings.

4.5.1 System Configuration Control registers summary

The base memory address of the SCC registers in the Morello SDP is 0x0_3FFF_F000 in the System Control Processor (SCP) SoC expansion region of the SCP memory map.

The following table shows the SCC registers in offset order from the base memory address. Undefined registers are reserved. Software must not attempt to access these registers.

Base memory address

0x0_3FFF_F000

Table 30: SCC registers summary

Offset	Name	Type	Reset	Width	Description
0x0004	PMCLK_DIV	RW/RO	0x0001_0001	32	See PMCLK_DIV Register.
0x000C	SYSAPBCLK_CTRL	RW/RO	0x0000_0101	32	See SYSAPBCLK_CTRL Register.
0x0010	SYSAPBCLK_DIV	RW/RO	0x0013_0013	32	See SYSAPBCLK_DIV Register.
0x0018	IOFPGA_TMIF2XCLK_CTRL	RW/RO	0x0000_0101	32	See IOFPGA_TMIF2XCLK_CTRL Register.
0x001C	IOFPGA_TMIF2XCLK_DIV	RW/RO	0x0000_0000	32	See IOFPGA_TMIF2XCLK_DIV Register.
0x0024	IOFPGA_TSIF2XCLK_CTRL	RW/RO	0x0000_0101	32	See IOFPGA_TSIF2XCLK_CTRL Register.
0x0028	IOFPGA_TSIF2XCLK_DIV	RW/RO	0x000B_000B	32	See IOFPGA_TSIF2XCLK_DIV Register.
0x0030	SCPNICCLK_CTRL	RW/RO	0x0000_0101	32	See SCPNICCLK_CTRL Register.

Offset	Name	Type	Reset	Width	Description
0x0034	SCPNICCLK_DIV	RW/RO	0x0000_0000	32	See SCPNICCLK_DIV Register .
0x003C	SCPI2CCLK_CTRL	RW/RO	0x0000_0101	32	See SCPI2CCLK_CTRL Register .
0x0040	SCPI2CCLK_DIV	RW/RO	0x000F_000F	32	See SCPI2CCLK_DIV Register .
0x0048	SCPQSPICLK_CTRL	RW/RO	0x0000_0101	32	See SCPQSPICLK_CTRL Register .
0x004C	SCPQSPICLK_DIV	RW/RO	0x0000_0000	32	See SCPQSPICLK_DIV Register .
0x0054	SENSORCLK_CTRL	RW/RO	0x0000_0101	32	See SENSORCLK_CTRL Register .
0x0058	SENSORCLK_DIV	RW/RO	0x0017_0017	32	See SENSORCLK_DIV Register .
0x0060	MCPNICCLK_CTRL	RW/RO	0x0000_0101	32	See MCPNICCLK_CTRL Register .
0x0064	MCPNICCLK_DIV	RW/RO	0x0000_0000	32	See MCPNICCLK_DIV Register .
0x006C	MCPI2CCLK_CTRL	RW/RO	0x0000_0101	32	See MCPI2CCLK_CTRL Register .
0x0070	MCPI2CCLK_DIV	RW/RO	0x0017_0017	32	See MCPI2CCLK_DIV Register .
0x0078	MCPQSPICLK_CTRL	RW/RO	0x0000_0101	32	See MCPQSPICLK_CTRL Register .
0x007C	MCPQSPICLK_DIV	RW/RO	0x0000_0000	32	See MCPQSPICLK_DIV Register .
0x0084	PCIEAXICLK_CTRL	RW/RO	0x0000_0101	32	See PCIEAXICLK_CTRL Register .
0x0088	PCIEAXICLK_DIV	RW/RO	0x0001_0001	32	See PCIEAXICLK_DIV Register .
0x0090	CCIXAXICLK_CTRL	RW/RO	0x0000_0101	32	See CCIXAXICLK_CTRL Register .

Offset	Name	Type	Reset	Width	Description
0x0094	CCIXAXICLK_DIV	RW/RO	0x0001_0001	32	See CCIXAXICLK_DIV Register .
0x009C	PCIEAPBCLK_CTRL	RW/RO	0x0000_0101	32	See PCIEAPBCLK_CTRL Register .
0x00A0	PCIEAPBCLK_DIV	RW/RO	0x000B_000B	32	See PCIEAPBCLK_DIV Register .
0x00A8	CCIXAPBCLK_CTRL	RW/RO	0x0000_0101	32	See CCIXAPBCLK_CTRL Register .
0x00AC	CCIXAPBCLK_DIV	RW/RO	0x000B_000B	32	See CCIXAPBCLK_DIV Register .
0x00F0	SYS_CLK_EN	RW	0x0000_3FF7	32	See SYS_CLK_EN Register .
0x0100	CPU0_PLL_CTRL0	RW	0x8010_3000	32	See CPU0_PLL_CTRL0 Register .
0x0104	CPU0_PLL_CTRL1	RW/RO	0x9100_0000	32	See CPU0_PLL_CTRL1 Register .
0x0108	CPU1_PLL_CTRL0	RW	0x8010_3000	32	See CPU1_PLL_CTRL0 Register .
0x010C	CPU1_PLL_CTRL1	RW/RO	0x9100_0000	32	See CPU1_PLL_CTRL1 Register .
0x0110	CLUS_PLL_CTRL0	RW	0x8010_2000	32	See CLUS_PLL_CTRL0 Register .
0x0114	CLUS_PLL_CTRL1	RW/RO	0x9100_0000	32	See CLUS_PLL_CTRL1 Register .
0x0118	SYS_PLL_CTRL0	RW	0x8010_3000	32	See SYS_PLL_CTRL0 Register .
0x011C	SYS_PLL_CTRL1	RW/RO	0x9100_0000	32	See SYS_PLL_CTRL1 Register .
0x0120	DMC_PLL_CTRL0	RW	0x8020_2000	32	See DMC_PLL_CTRL0 Register .
0x0124	DMC_PLL_CTRL1	RW/RO	0x9100_0000	32	See DMC_PLL_CTRL1 Register .

Offset	Name	Type	Reset	Width	Description
0x0128	INT_PLL_CTRL0	RW	0x8010_2000	32	See INT_PLL_CTRL0 Register .
0x012C	INT_PLL_CTRL1	RW/RO	0x9100_0000	32	See INT_PLL_CTRL1 Register .
0x0130	GPU_PLL_CTRL0	RW	-	32	See GPU_PLL_CTRL0 Register .
0x0134	GPU_PLL_CTRL1	RW/RO	-	32	See GPU_PLL_CTRL1 Register .
0x0138	DPU_PLL_CTRL0	RW	-	32	See DPU_PLL_CTRL0 Register .
0x013C	DPU_PLL_CTRL1	RW/RO	-	32	See DPU_PLL_CTRL1 Register .
0x0140	PXL_PLL_CTRL0	RW	-	32	See PXL_PLL_CTRL0 Register .
0x0144	PXL_PLL_CTRL1	RW/RO	-	32	See PXL_PLL_CTRL1 Register .
0x0150	SYS_MAN_RESET	RW	0x0000_0C00	32	See SYS_MAN_RESET Register .
0x0160	BOOT_CTL	RW/RO	0x0000_0000	32	See BOOT_CTL Register .
0x0164	BOOT_CTRL_STA	RW/RO	0x0000_0000	32	See BOOT_CTRL_STA Register .
0x0168	SCP_BOOT_ADR	RW/RO	0x0000_0000	32	See SCP_BOOT_ADR Register .
0x016C	MCP_BOOT_ADR	RW/RO	0x0000_0000	32	See MCP_BOOT_ADR Register .
0x0170	PLATFORM_CTRL	RW/RO	0x0000_0000	32	See PLATFORM_CTRL Register .
0x0174	TARGETIDAPP	RW/RO	0x07B3_0477	32	See TARGETIDAPP Register .
0x0178	TARGETIDSCP	RW/RO	0x07B5_0477	32	See TARGETIDSCP Register .
0x017C	TARGETIDMCP	RW/RO	0x07B4_0477	32	See TARGETIDMCP Register .

Offset	Name	Type	Reset	Width	Description
0x0180	BOOT_GPR0	RW/RO	0x0000_0000	32	See BOOT_GPR0 Register .
0x0184	BOOT_GPR1	RW/RO	0x0000_0000	32	See BOOT_GPR1 Register .
0x0188	BOOT_GPR2	RW/RO	0x0000_0000	32	See BOOT_GPR2 Register .
0x018C	BOOT_GPR3	RW/RO	0x0000_0000	32	See BOOT_GPR3 Register .
0x0190	BOOT_GPR4	RW/RO	0x0000_0000	32	See BOOT_GPR4 Register .
0x0194	BOOT_GPR5	RW/RO	0x0000_0000	32	See BOOT_GPR5 Register .
0x0198	BOOT_GPR6	RW/RO	0x0000_0000	32	See BOOT_GPR6 Register .
0x019C	BOOT_GPR7	RW/RO	0x0000_0000	32	See BOOT_GPR7 Register .
0x01A0	INSTANCE_ID	RW/RO	0x0000_0000	32	See INSTANCE_ID Register .
0x01A4	PCIE_BOOT_CTRL	RW	0x0000_0003	32	See PCIE_BOOT_CTRL Register .
0x01AC	GPU_CTRL	RW	0x0000_0018	32	See GPU_CTRL Register .
0x01B4	DBG_AUTHN_CTRL	RW	0x0000_0007	32	See DBG_AUTHN_CTRL Register .
0x01B8	CTI0_CTRL	RW	0x0000_0000	32	See CTI0_CTRL Register .
0x01BC	CTI1_CTRL	RW	0x0000_0000	32	See CTI1_CTRL Register .
0x01C0	CTI0TO3_CTRL	RW	0x0000_0000	32	See CTI0TO3_CTRL Register .
0x01C4	MCP_WDOGCTI_CTRL	RW	0x0000_0000	32	See MCP_WDOGCTI_CTRL Register .
0x01C8	SCP_WDOGCTI_CTRL	RW	0x0000_0000	32	See SCP_WDOGCTI_CTRL Register .
0x01CC	DBGEXPCTI_CTRL	RW	0x0000_0000	32	See DBGEXPCTI_CTRL Register .
0x01D0	PCIE_PM_CTRL	RW/RO	0x0000_0000	32	See PCIE_PM_CTRL Register .

Offset	Name	Type	Reset	Width	Description
0x01D4	CCIX_PM_CTRL	RW/RO	0x0000_0000	32	See CCIX_PM_CTRL Register .
0x01D8	SCDBG_CTRL	RW/RO	0x0000_0000	32	See SCDBG_CTRL Register .
0x01DC	EXP_IF_CTRL	RW	0x0000_0000	32	See EXP_IF_CTRL Register .
0x01E4	RO_CTRL	RW	0x0000_0001	32	See RO_CTRL Register .
0x01E8	CMN_CCIX_CTRL	RW/RO	0x0101_0000	32	See CMN_CCIX_CTRL Register .
0x01EC	STM_CTRL	RW	0x0000_0000	32	See STM_CTRL Register .
0x01F0	AXI_OVRD_PCIE	RW	0x0030_3030	32	See AXI_OVRD_PCIE Register .
0x01F4	AXI_OVRD_CCIX	RW	0x0030_3030	32	See AXI_OVRD_CCIX Register .
0x01F8	AXI_OVRD_TSIF	RW	0x0000_3030	32	See AXI_OVRD_TSIF Register .
0x01FC	GPU_TEXFMTENABLE	RW	0x0000_0000	32	See GPU_TEXFMTENABLE Register .
0x0200	TRACE_PAD_CTRL0	RW	0x1111_1111	32	See TRACE_PAD_CTRL0 Register .
0x0204	TRACE_PAD_CTRL1	RW	0x0000_1111	32	See TRACE_PAD_CTRL1 Register .
0x0208	IOFPGA_TMIF_PAD_CTRL	RW	0x0011_1111	32	See IOFPGA_TMIF_PAD_CTRL Register .
0x020C	IOFPGA_TSIF_PAD_CTRL	RW	0x0011_1111	32	See IOFPGA_TSIF_PAD_CTRL Register .
0x0210	DISPLAY_PAD_CTRL0	RW	0x0101_0101	32	See DISPLAY_PAD_CTRL0 Register .
0x0214	DISPLAY_PAD_CTRL1	RW	0x0101_0101	32	See DISPLAY_PAD_CTRL1 Register .
0x0E00	APB_CTRL_CLR	RO	0x0000_0000	32	See APB_CTRL_CLR Register .

Offset	Name	Type	Reset	Width	Description
0x0FD0	PID4	RO	0x0000_0004	32	See PID4 Register .
0xFE0	PID0	RO	0x0000_00AF	32	See PID0 Register .
0xFE4	PID1	RO	0x0000_00B0	32	See PID1 Register .
0xFE8	PID2	RO	0x0000_000B	32	See PID2 Register .
0xFEC	PID3	RO	0x0000_0000	32	See PID3 Register .
0xFF0	CID0	RO	0x0000_000D	32	See CID0 Register .
0xFF4	CID1	RO	0x0000_00F0	32	See CID1 Register .
0xFF8	CID2	RO	0x0000_0005	32	See CID2 Register .
0xFFC	CID3	RO	0x0000_00B1	32	See CID3 Register .

4.5.2 PMCLK_DIV Register

The PMCLK_DIV Register characteristics are:

Purpose

Controls the **PMCLK** division value from **REFCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PMCLK_DIV Register bit assignments.

Table 31: PMCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKSEL_CUR+1. Reset value 0b00001, division value=2.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKSEL_CUR+1. Reset value 0b00001, division value=2.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.3 SYSAPBCLK_CTRL Register

The SYSAPBCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **SYSAPBCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SYSAPBCLK_CTRL Register bit assignments.

Table 32: SYSAPBCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for SYSAPBCLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for SYSAPBCLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0010.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.4 SYSAPBCLK_DIV Register

The SYSAPBCLK_DIV Register characteristics are:

Purpose

Controls the **SYSAPBCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SYSAPBCLK_DIV Register bit assignments.

Table 33: SYSAPBCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value =CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value =CLKDIV_CUR+1. Reset value 0b10011, division value=20.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.5 IOFPGA_TMIF2XCLK_CTRL Register

The IOFPGA_TMIF2XCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **TMIF2XCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the IOFPGA_TMIF2XCLK_CTRL Register bit assignments.

Table 34: IOFPGA_TMIF2XCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for TMIF2XCLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for TMIF2XCLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0010.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.6 IOFPGA_TMIF2XCLK_DIV Register

The IOFPGA_TMIF2XCLK_DIV Register characteristics are:

Purpose

Controls the TMIF2XCLK division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the IOFPGA_TMIF2XCLK_DIV Register bit assignments.

Table 35: IOFPGA_TMIF2XCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b10011, division value=20.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.7 IOFPGA_TSIF2XCLK_CTRL Register

The IOFPGA_TSIF2XCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **TSIF2XCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the IOFPGA_TSIF2XCLK_CTRL Register bit assignments.

Table 36: IOFPGA_TSIF2XCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for TSIF2XCLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for TSIF2XCLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0010.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.8 IOFPGA_TSIF2XCLK_DIV Register

The IOFPGA_TSIF2XCLK_DIV Register characteristics are:

Purpose

Controls the TSIF2XCLK division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the IOFPGA_TSIF2XCLK_DIV Register bit assignments.

Table 37: IOFPGA_TSIF2XCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b10011, division value=20.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.9 SCPNICCLK_CTRL Register

The SCPNICCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **SCPNICCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SCPNICCLK_CTRL Register bit assignments.

Table 38: SCPNICCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for SCPNICCLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for SCPNICCLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0010.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.10 SCPNICCLK_DIV Register

The SCPNICCLK_DIV Register characteristics are:

Purpose

Controls the **SCPNICCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SCPNICCLK_DIV Register bit assignments.

Table 39: SCPNICCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b00111, division value=8.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.11 SCPI2CCLK_CTRL Register

The SCPI2CCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **SCPI2CCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SCPI2CCLK_CTRL Register bit assignments.

Table 40: SCPI2CCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for SCPI2CCLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RO	Select source for SCPI2CCLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0001.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.12 SCPI2CCLK_DIV Register

The SCPI2CCLK_DIV Register characteristics are:

Purpose

Controls the **SCPI2CCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SCPI2CCLK_DIV Register bit assignments.

Table 41: SCPI2CCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1 Reset value 0b00000, division value = 1.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.13 SCPQSPICLK_CTRL Register

The SCPQSPICLK_CTRL Register characteristics are:

Purpose

Selects source for clock **SCPQSPICLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SCPQSPICLK_CTRL Register bit assignments.

Table 42: SCPQSPICLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for SCPQSPICLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for SCPQSPICLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0001.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.14 SCPQSPICLK_DIV Register

The SCPQSPICLK_DIV Register characteristics are:

Purpose

Controls the **SCPQSPICLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SCPQSPICLK_DIV Register bit assignments.

Table 43: SCPQSPICLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value =CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value =CLKDIV_CUR+1. Reset value 0b00000, division value=1.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.15 SENSORCLK_CTRL Register

The SENSORCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **SENSORCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SENSORCLK_CTRL Register bit assignments.

Table 44: SENSORCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for SENSORCLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for SENSORCLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0010.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.16 SENSORCLK_DIV Register

The SENSORCLK_DIV Register characteristics are:

Purpose

Controls the **SENSORCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SENSORCLK_DIV Register bit assignments.

Table 45: SENSORCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b10111, division value = 24.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.17 MCPNICCLK_CTRL Register

The MCPNICCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **MCPNICCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the MCPNICCLK_CTRL Register bit assignments.

Table 46: MCPNICCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for MCPNICCLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for MCPNICCLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0010.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.18 MCPNICCLK_DIV Register

The MCPNICCLK_DIV Register characteristics are:

Purpose

Controls the **MCPNICCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the MCPNICCLK_DIV Register bit assignments.

Table 47: MCPNICCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b00111, division value = 8.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.19 MCPI2CCLK_CTRL Register

The MCPI2CCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **MCPI2CCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the MCPI2CCLK_CTRL Register bit assignments.

Table 48: MCPI2CCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for MCPI2CCLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for MCPI2CCLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0001.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.20 MCPI2CCLK_DIV Register

The MCPI2CCLK_DIV Register characteristics are:

Purpose

Controls the **MCPI2CCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the MCPI2CCLK_DIV Register bit assignments.

Table 49: MCPI2CCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b00000, division value = 1.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.21 MCPQSPICLK_CTRL Register

The MCPQSPICLK_CTRL Register characteristics are:

Purpose

Selects source for clock **MCPQSPICLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the MCPQSPICLK_CTRL Register bit assignments.

Table 50: MCPQSPICLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for MCPQSPICLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for MCPQSPICLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0001.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.22 MCPQSPICLK_DIV Register

The MCPQSPICLK_DIV Register characteristics are:

Purpose

Controls the MCPQSPICLK division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the MCPQSPICLK_DIV Register bit assignments.

Table 51: MCPQSPICLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b00000, division value = 1.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.23 PCIEAXICKL_CTRL Register

The PCIEAXICKL_CTRL Register characteristics are:

Purpose

Selects source for clock **PCIEAXICKL**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PCIEAXICKL_CTRL Register bit assignments.

Table 52: PCIEAXICKL_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for PCIEAXICK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for PCIEAXICK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0010.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.24 PCIEAXICK_DIV Register

The PCIEAXICK_DIV Register characteristics are:

Purpose

Controls the **PCIEAXICK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PCIEAXICK_DIV Register bit assignments.

Table 53: PCIEAXICK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b00001, division value = 2.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.25 CCIXAXICKL_CTRL Register

The CCIXAXICKL_CTRL Register characteristics are:

Purpose

Selects source for clock **CCIXAXICKL**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CCIXAXICKL_CTRL Register bit assignments.

Table 54: CCIXAXICKL_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for CCIXAXICLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for CCIXAXICLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0010.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.26 CCIXAXICLK_DIV Register

The CCIXAXICLK_DIV Register characteristics are:

Purpose

Controls the **CCIXAXICLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CCIXAXICLK_DIV Register bit assignments.

Table 55: CCIXAXICLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b00001, division value = 2.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.27 PCIEAPBCLK_CTRL Register

The PCIEAPBCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **PCIEAPBCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PCIEAPBCLK_CTRL Register bit assignments.

Table 56: PCIEAPBCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for PCIEAPBCLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for PCIEAPBCLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0010.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.28 PCIEAPBCLK_DIV Register

The PCIEAPBCLK_DIV Register characteristics are:

Purpose

Controls the **PCIEAPBCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PCIEAPBCLK_DIV Register bit assignments.

Table 57: PCIEAPBCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b01011, division value = 12.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.29 CCIXAPBCLK_CTRL Register

The CCIXAPBCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **CCIXAPBCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CCIXAPBCLK_CTRL Register bit assignments.

Table 58: CCIXAPBCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.

Bits	Name	Type	Function
[11:8]	CLKSEL_CUR	RO	Current value of source for CCIXAPBCLK : 0b0001: Source is REFCLK . 0b0010: Source is divided SYSPLLCLK .
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for CCIXAPBCLK : 0b0001: Select REFCLK . 0b0010: Select divided SYSPLLCLK . Reset value 0b0010.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.30 CCIXAPBCLK_DIV Register

The CCIXAPBCLK_DIV Register characteristics are:

Purpose

Controls the **CCIXAPBCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CCIXAPBCLK_DIV Register bit assignments.

Table 59: CCIXAPBCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value = CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value = CLKDIV_CUR+1. Reset value 0b01011, division value = 12.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.31 SYS_CLK_EN Register

The SYS_CLK_EN Register characteristics are:

Purpose

Enables or disables internally generated clocks.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SYS_CLK_EN Register bit assignments.

Table 60: SYS_CLK_EN Register bit assignments

Bits	Name	Type	Function
[31:14]	-	-	Reserved.

Bits	Name	Type	Function
[13]	CCIXAPBCLKEN	RW	Enable clock CCIXAPBCLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.
12	CCIXAXICLKEN	RW	Enable clock CCIXAXICLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.
11	PCIEAPBCLKEN	RW	Enable clock PCIEAPBCLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.
10	PCIEAXICLKEN	RW	Enable clock PCIEAXICLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.
9	MCPQSPICLKEN	RW	Enable clock MCPQSPICLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.
8	MCPI2CCLKEN	RW	Enable clock MCPI2CCLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.

Bits	Name	Type	Function
7	MCPNICCLKEN	RW	Enable clock MCPNICCLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.
6	SENSORCLKEN	RW	Enable clock SENSORCLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.
5	SCPQSPICLKEN	RW	Enable clock SCPQSPICLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.
4	SCPI2CCLKEN	RW	Enable clock SCPI2CCLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.
3	-	-	Reserved.
2	IOFP GA_TSIF2XCLKEN	RW	Enable clock TSIF2XCLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.
1	IOFP GA_TMIF2XCLKEN	RW	Enable clock TMIF2XCLK : 0b0: Clock disabled. 0b1: Clock enabled. Reset value 0b1.

Bits	Name	Type	Function
0	SYSAPBCLKEN	RW	<p>Enable clock SYSAPBCLK:</p> <p>0b0: Clock disabled.</p> <p>0b1: Clock enabled.</p> <p>Reset value 0b1.</p>

4.5.32 CPU0_PLL_CTRL0 Register

The CPU0_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register CPU0_PLL_CTRL1, control the settings of clock control PLL CPU0PLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CPU0_PLL_CTRL0 Register bit assignments.

Table 61: CPU0_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	<p>PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to 0b1:</p> <p>0x0: PLL disabled.</p> <p>0x1: PLL disabled.</p> <p>Reset value 0x1.</p>
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	<p>PLL reference, input clock, divider value.</p> <p>Reset value 0b1.</p>

Bits	Name	Type	Function
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value 0x30 , division value=48.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS	RW	Bypasses PLL to drive input clock directly into the SoC: 0x0: PLL not bypassed. 0x1: PLL bypassed. Reset value 0b0.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.33 CPU0_PLL_CTRL1 Register

The CPU0_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register CPU0_PLL_CTRL0, control the settings of clock control PLL CPU0PLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CPU0_PLL_CTRL1 Register bit assignments.

Table 62: CPU0_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.

Bits	Name	Type	Function
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value 0b1.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value 0b1.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction =FRAC/2 ²⁴ . Reset value 0x0.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.34 CPU1_PLL_CTRL0 Register

The CPU1_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register CPU1_PLL_CTRL1, control the settings of clock control PLL CPU1PLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CPU1_PLL_CTRL0 Register bit assignments.

Table 63: CPU1_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to 0b1: 0x0: PLL disabled. 0x1: PLL enabled . Reset value 0x1.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value 0b1.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value 0x30 , division value=48.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS	RW	Bypasses PLL to drive input clock directly into the SoC: 0x0: PLL not bypassed. 0x1: PLL bypassed. Reset value 0b0.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.35 CPU1_PLL_CTRL1 Register

The CPU1_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register CPU1_PLL_CTRL0, control the settings of clock control PLL CPU1PLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CPU1_PLL_CTRL1 Register bit assignments.

Table 64: CPU1_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value 0b1.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value 0b1.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction = $\text{FRAC}/2^{24}$. Reset value 0x0.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.36 CLUS_PLL_CTRL0 Register

The CLUS_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register CLUS_PLL_CTRL1, control the settings of clock control PLL CLUSPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CLUS_PLL_CTRL0 Register bit assignments.

Table 65: CLUS_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to 0b1: 0b0: PLL disabled. 0b1: PLL enable. Reset value 0x1.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value 0b1.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value 0x20 , division value=32.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS		Bypasses PLL to drive input clock directly into the SoC: 0b0: PLL not bypassed.. 0b1: PLL bypassed. Reset value 0b0.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.37 CLUS_PLL_CTRL1 Register

The CLUS_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register CLUS_PLL_CTRL0, control the settings of clock control PLL CLUSPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CLUS_PLL_CTRL1 Register bit assignments.

Table 66: CLUS_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value 0b1.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value 0b1.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction = $\text{FRAC}/2^{24}$. Reset value 0x0.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.38 SYS_PLL_CTRL0 Register

The SYS_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register SYS_PLL_CTRL1, control the settings of clock control PLL SYSPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SYS_PLL_CTRL0 Register bit assignments.

Table 67: SYS_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to 0b1: 0b0: PLL disabled. 0b1: PLL enabled Reset value 0x1.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value 0b1.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value 0x30, division value=48.
[7:1]	-	-	Reserved.

Bits	Name	Type	Function
[0]	HARD_BYPASS		<p>Bypasses PLL to drive input clock directly into the SoC:</p> <p>0b0: PLL not bypassed.</p> <p>0b1: PLL bypassed.</p> <p>Reset value 0b0.</p>



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.39 SYS_PLL_CTRL1 Register

The SYS_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register SYS_PLL_CTRL0, control the settings of clock control PLL SYSSPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SYS_PLL_CTRL1 Register bit assignments.

Table 68: SYS_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	<p>Second post-divide value.</p> <p>Post-divide value=POSTDIV2.</p> <p>Reset value 0b1.</p>
[27]	-	-	Reserved.

Bits	Name	Type	Function
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value 0b1.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction $\text{FRAC}/2^{24}$. Reset value 0x0.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.40 DMC_PLL_CTRL0 Register

The DMC_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register DMC_PLL_CTRL1, control the settings of clock control PLL DMCPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the DMC_PLL_CTRL0 Register bit assignments.

Table 69: DMC_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to 0b1: 0b0: PLL disabled. 0b1: PLL enabled . Reset value 0x1.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock divider value. Reset value 0b1.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value 0x20 , division value=32.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS	RW	Bypasses PLL to drive input clock directly into the SoC: 0b0: PLL not bypassed. 0b1: PLL bypassed. Reset value 0b0.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.41 DMC_PLL_CTRL1 Register

The DMC_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register DMC_PLL_CTRL0, control the settings of clock control PLL DMCPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the DMC_PLL_CTRL1 Register bit assignments.

Table 70: DMC_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value 0b1.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value 0b1.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction = $\text{FRAC}/2^{24}$. Reset value 0x0.



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.42 INT_PLL_CTRL0 Register

The INT_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register INT_PLL_CTRL1, control the settings of clock control PLL INTPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the INT_PLL_CTRL0 Register bit assignments.

Table 71: INT_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to 0b1: 0b0: PLL disabled. 0b1: PLL enabled . Reset value 0b0.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value 0b1.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value 0x20 , division value = 32.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS	-	Bypasses PLL to drive input clock directly into the SoC: 0b0: PLL not bypassed. 0b1: PLL bypassed. Reset value 0b0.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.43 INT_PLL_CTRL1 Register

The INT_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register INT_PLL_CTRL0, control the settings of clock control PLL INTPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the INT_PLL_CTRL1 Register bit assignments.

Table 72: INT_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value 0b1.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value 0b1.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction = $\text{FRAC}/2^{24}$



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.44 GPU_PLL_CTRL1 Register

The GPU_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register GPU_PLL_CTRL0, control the settings of clock control PLL GPUPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the GPU_PLL_CTRL1 Register bit assignments.

Table 73: GPU_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value 0x1.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value 0x2.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction =FRAC/2 ²⁴ .



Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.45 GPU_PLL_CTRL0 Register

The INT_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register GPU_PLL_CTRL1, control the settings of clock control PLL GPUPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the GPU_PLL_CTRL0 Register bit assignments.

Table 74: GPU_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to 1: 0: PLL disabled. 1: PLL enabled. Reset value 0x0.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value 0x1.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value 0x1A, division value=32.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS		Bypasses PLL to drive input clock directly into the SoC: 0: PLL not bypassed. 1: PLL bypassed. Reset value 0x0.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.46 DPU_PLL_CTRL1 Register

The DPU_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register DPU_PLL_CTRL0, control the settings of clock control PLL DPUPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the DPU_PLL_CTRL1 Register bit assignments.

Table 75: DPU_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value 0x1.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value 0x5.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction = $\text{FRAC}/2^{24}$.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.47 DPU_PLL_CTRL0 Register

The DPU_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register DPU_PLL_CTRL1, control the settings of clock control PLL DPUPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the DPU_PLL_CTRL0 Register bit assignments.

Table 76: DPU_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to 1: 0: PLL disabled. 1: PLL enabled. Reset value 0x0.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value 0x2.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value 0x49 , division value=32.
[7:1]	-	-	Reserved.

Bits	Name	Type	Function
[0]	HARD_BYPASS		Bypasses PLL to drive input clock directly into the SoC: 0: PLL not bypassed. 1: PLL bypassed. Reset value 0x0.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.48 PXL_PLL_CTRL1 Register

The PXL_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register PXL_PLL_CTRL0, control the settings of clock control PLL PXLPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PXL_PLL_CTRL1 Register bit assignments.

Table 77: PXL_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value 0x1.
[27]	-	-	Reserved.

Bits	Name	Type	Function
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value 0x5.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction = $\text{FRAC}/2^{24}$.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.49 PXL_PLL_CTRL0 Register

The PXL_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register PXL_PLL_CTRL1, control the settings of clock control PLL PXLPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PXL_PLL_CTRL0 Register bit assignments.

Table 78: PXL_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to 1: 0: PLL disabled. 1: PLL enabled. Reset value 0x0.

Bits	Name	Type	Function
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value 0x5.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value 0x51 , division value=32.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS		Bypasses PLL to drive input clock directly into the SoC: 0: PLL not bypassed. 1: PLL bypassed. Reset value 0x0.



The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the Morello SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.50 SYS_MAN_RESET Register

The SYS_MAN_RESET Register characteristics are:

Purpose

Controls the manual resets of the internal resets at SoC level.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SYS_MAN_RESET Register bit assignments.

Table 79: SYS_MAN_RESET Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11]	FORCE_CCIX_APB_RST	RW	CCIX APB reset, CCIX top reset: 0b0: Not reset. 0b1: Reset. Reset value 0b1.
[10]	FORCE_PCIE_APB_RST	-	PCIe APB reset, PCIe top reset: 0b0: Not reset. 0b1: Reset. Reset value 0b1.
[9:8]	-	-	Reserved.
[7]	FORCE_MCP_QSPI_RST	-	MCPQSPICLK manual reset: 0b0: Not reset. 0b1: Reset. Reset value 0b0.
[6]	FORCE_MCP_I2C_RST	-	MCP I2CCLK clock manual reset: 0b0: Not reset. 0b1: Reset. Reset value 0b0.
[5]	FORCE_S_CP_SENSOR_RST	-	SENSORCLK manual reset: 0b0: Not reset. 0b1: Reset. Reset value 0b0.

Bits	Name	Type	Function
[4]	FORCE_SCP_QSPI_RST	-	SCPQSPICLK manual reset: 0b0: Not reset. 0b1: Reset. Reset value 0b0.
[3]	FORCE_SCP_I2C_RST	-	SCP I2CCLK manual reset: 0b0: Not reset. 0b1: Reset. Reset value 0b0.
[2]	FORCE_IO_FPGA_TSIF_RST	-	TSIF2XCLK manual reset: 0b0: Not reset. 0b1: Reset. Reset value 0b0.
[1]	FORCE_IO_FPGA_TMIF_RST	-	TMIF2XCLK manual reset: 0b0: Not reset. 0b1: Reset. Reset value 0b0.
[0]	FORCE_SYS_APB_RST	-	SYSAPBCLK manual reset: 0b0: Not reset. 0b1: Reset. Reset value 0b0.

4.5.51 BOOT_CTL Register

The BOOT_CTL Register characteristics are:

Purpose

Controls powerup reset hold and MSCP bootup type.

Usage constraints

This register is read-only from APB interface and read/write from serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the BOOT_CTL Register bit assignments.

Table 80: BOOT_CTL Register bit assignments

Bits	Name	Type	Function
[31]	PORESET_HOLD	RO from APB interface. RW from serial interface.	Powerup reset hold: 0b0: Do not hold powerup reset. 0b1: Hold poweru p reset. Reset value 0b0. This bit is valid only when MSCP_BOOT_TYPE=1 .
[30:1]	-		Reserved.
[0]	MSCP_BOOT_TYPE	RO from APB interface. RW from serial interface.	MSCP bootup type: 0b0: Boot from QSPI. 0b1: Boot from TLX master interface. Reset value 0b0.

4.5.52 BOOT_CTRL_STA Register

The BOOT_CTRL_STA Register characteristics are:

Purpose

Stores bootup statuses.

Usage constraints

Bits[31:24] are read/write. Bits[6:0] are read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the BOOT_CTRL_STA Register bit assignments.

Table 81: BOOT_CTRL_STA Register bit assignments

Bits	Name	Type	Function
[31:24]	MSCP_BOOT_STATUS	RW	SCP can use this field to store MSCP bootup status for MCC to read. Reset value 0x00.
[23:7]	-	-	Reserved.
[6]	MCP_ACG_QDENY	RO	MCP ACG QDENYn . Reset value 0b0.
[5]	MCP_ACG_QACCEPT	RO	MCP ACG QACCEPTn . Reset value 0b0.
[4]	MCP_QACTIVE	RO	MCP ACG QACTIVE . Reset value 0b0.
[3]	-	RO	Reserved.
[2]	SCP_ACG_QDENY	RO	SCP ACG QDENYn .
[1]	SCP_QACCEPT	RO	SCP ACG QACCEPTn . Reset value 0b0.
[0]	SCP_ACG_QACTIVE	RO	SCP ACG QACTIVE . Reset value 0b0.

4.5.53 SCP_BOOT_ADR Register

The SCP_BOOT_ADR Register characteristics are:

Purpose

Stores the SCP bootup address.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SCP_BOOT_ADR Register bit assignments.

Table 82: SCP_BOOT_ADR Register bit assignments

Bits	Name	Type	Function
[31:0]	ADDRESS	RO from APB interface. RW from serial interface.	Bootup address of SCP. Reset value 0x00000000.

4.5.54 MCP_BOOT_ADR Register

The MCP_BOOT_ADR Register characteristics are:

Purpose

Stores the MCP bootup address.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the MCP_BOOT_ADR Register bit assignments.

Table 83: MCP_BOOT_ADR Register bit assignments

Bits	Name	Type	Function
[31:0]	ADDRESS	RO from APB interface. RW from serial interface.	Bootup address of MCP. Reset value 0x00000000.

4.5.55 PLATFORM_CTRL Register

The PLATFORM_CTRL Register characteristics are:

Purpose

Morello SoC platform control.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PLATFORM_CTRL Register bit assignments.

Table 84: PLATFORM_CTRL Register bit assignments

Bits	Name	Type	Function
[31:9]	-	-	Reserved.
[8]	MULTI_CHIP_MODE	RO from APB interface. RW from serial interface.	Multi-chip tie-off value: 0b0: Single chip. 0b1: Multi-chip. Reset value 0b0.
[7:6]	-	-	Reserved.
[5:0]	CHIPID	RO from APB interface. RW from serial interface.	CHIP ID tie-off value in multichip mode. This value is 0b00000 for single chip mode.

4.5.56 TARGETIDAPP Register

The TARGETIDAPP Register characteristics are:

Purpose

CoreSight target ID of Application Processor (AP).

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the TARGETIDAPP Register bit assignments.

Table 85: TARGETIDAPP Register bit assignments

Bits	Name	Type	Function
[31:0]	ID	RO from APB interface. RW from serial interface.	CoreSight target ID of AP. Reset value 0x07B30477.

4.5.57 TARGETIDSCP Register

The TARGETIDSCP Register characteristics are:

Purpose

Stores the SCP bootup address.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SCP_BOOT_ADR Register bit assignments.

Table 86: SCP_BOOT_ADR Register bit assignments

Bits	Name	Type	Function
[31:0]	ID	RO from APB interface. RW from serial interface.	CoreSight target ID of SCP. Reset value 0x07B40477.

4.5.58 TARGETIDMCP Register

The TARGETIDMCP Register characteristics are:

Purpose

Stores the MCP bootup address.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the TARGETIDMCP Register bit assignments.

Table 87: TARGETIDMCP Register bit assignments

Bits	Name	Type	Function
[31:0]	ID	RO from APB interface. RW from serial interface.	CoreSight target ID of MCP. Reset value 0x07B50477.

4.5.59 BOOT_GPR0 Register

The BOOT_GPR0 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the Morello SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the BOOT_GPR0 Register bit assignments.

Table 88: BOOT_GPR0 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 0. Reset value 0x00000000.

4.5.60 BOOT_GPR1 Register

The BOOT_GPR1 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the Morello SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the BOOT_GPR1 Register bit assignments.

Table 89: BOOT_GPR1 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 1. Reset value 0x00000000.

4.5.61 BOOT_GPR2 Register

The BOOT_GPR2 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the Morello SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the BOOT_GPR2 Register bit assignments.

Table 90: BOOT_GPR2 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 2. Reset value 0x00000000.

4.5.62 BOOT_GPR3 Register

The BOOT_GPR3 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the Morello SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the BOOT_GPR3 Register bit assignments.

Table 91: BOOT_GPR3 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 3. Reset value 0x00000000.

4.5.63 BOOT_GPR4 Register

The BOOT_GPR4 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the Morello SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the BOOT_GPR4 Register bit assignments.

Table 92: BOOT_GPR4 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 4. Reset value 0x00000000.

4.5.64 BOOT_GPR5 Register

The BOOT_GPR5 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the Morello SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the BOOT_GPR5 Register bit assignments.

Table 93: BOOT_GPR5 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 5. Reset value 0x00000000.

4.5.65 BOOT_GPR6 Register

The BOOT_GPR6 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the Morello SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the BOOT_GPR6 Register bit assignments.

Table 94: BOOT_GPR6 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 6. Reset value 0x00000000.

4.5.66 BOOT_GPR7 Register

The BOOT_GPR7 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the Morello SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the BOOT_GPR7 Register bit assignments.

Table 95: BOOT_GPR7 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 7. Reset value 0x00000000.

4.5.67 INSTANCE_ID Register

The INSTANCE_ID Register characteristics are:

Purpose

SWJ-DP instance ID register.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the INSTANCE_ID Register bit assignments.

Table 96: INSTANCE_ID Register bit assignments

Bits	Name	Type	Function
[31:4]	-	-	Reserved.
[3:0]	ID	RO from APB interface. RW from serial interface.	SWJ-DP instance ID register. Reset value 0b0000.

4.5.68 PCIE_BOOT_CTRL Register

The PCIE_BOOT_CTRL Register characteristics are:

Purpose

Enables reset of sticky bits in the PCIe and CCIX controllers during reset of the PCIe and CCIX controllers.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PCIE_BOOT_CTRL Register bit assignments.

Table 97: PCIE_BOOT_CTRL Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1]	CCIX_STICKY_RST_EN	RW	Enable reset of all sticky bits in the CCIX controller during CCIX controller reset: 0b0: Not enable reset of sticky bits. 0b1: Enable reset of sticky bits . Reset value 0b1.
[0]	PCIE_STICKY_RST_EN	RW	Enable reset of all sticky bits in the PCIe controller during PCIe controller reset: 0b0: Not enable reset of sticky bits. 0b1: Enable reset of sticky bits . Reset value 0b1.

4.5.69 GPU_CTRL Register

The GPU_CTRL Register characteristics are:

Purpose

GPU control register.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the GPU_CTRL Register bit assignments.

Table 98: GPU_CTRL Register bit assignments

Bits	Name	Type	Function
[31:5]	-	-	Reserved.
[4]	GPU_NIDEN	RW	Non-invasive debug enable. Reset value 0x1.
[3]	GPU_DBGEN	RW	Debug enable. Reset value 0x1.
[2:0]	GPU_STRIPING_GRANULE	RW	4KB Norr L2 cache granule size. Reset value 0x0.

4.5.70 DBG_AUTHN_CTRL Register

The DBG_AUTHN_CTRL Register characteristics are:

Purpose

Drives the CoreSight™ authentication external interface.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the DBG_AUTHN_CTRL Register bit assignments.

Table 99: DBG_AUTHN_CTRL Register bit assignments

Bits	Name	Type	Function
[31:3]	-	-	Reserved.
[2]	DBG_SPNIDEN	RW	Secure non-invasive debug enable: 0b0: Disable. 0b1: Enable. Reset value 0b1.
[1]	DBG_SPIDEN	RW	Secure invasive debug enable: 0b0: Disable. 0b1: Enable. Reset value 0b1.
[0]	DBG_DEVICEEN	RW	Global external debug enable: 0b0: Disable. 0b1: Enable. Reset value 0b1.

4.5.71 CTIO_CTRL Register

The CTIO_CTRL Register characteristics are:

Purpose

CTI trigger mask register.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CTIO_CTRL Register bit assignments.

Table 100: CTI0_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:8]	TODBGENSEL	RW	CTI TODBGENSEL input. Reset value 0x00 .
[7:0]	TINIDENSEL	RW	CTI TINIDENSEL input. Reset value 0x0.

4.5.72 CTI1_CTRL Register

The CTI1_CTRL Register characteristics are:

Purpose

CTI trigger mask register.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CTI1_CTRL Register bit assignments.

Table 101: CTI1_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:8]	TODBGENSEL	RW	CTI TODBGENSEL input. Reset value 0x00 .
[7:0]	TINIDENSEL	RW	CTI TINIDENSEL input. Reset value 0x0.

4.5.73 CTI0TO3_CTRL Register

The CTI0TO3_CTRL Register characteristics are:

Purpose

CTI trigger mask register.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CTI0TO3_CTRL Register bit assignments.

Table 102: CTI0TO3_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:8]	TODBGENSEL	RW	CTI TODBGENSEL input. Reset value 0x00 .
[7:0]	TINIDENSEL	RW	CTI TINIDENSEL input. Reset value 0x00 .

4.5.74 MCP_WDOGCTI_CTRL Register

The MCP_WDOGCTI_CTRL Register characteristics are:

Purpose

CTI trigger mask register.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the MCP_WDOGCTI_CTRL Register bit assignments.

Table 103: MCP_WDOGCTI_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:8]	TODBGENSEL	RW	CTI TODBGENSEL input. Reset value 0x00 .
[7:0]	-	-	Reserved.

4.5.75 SCP_WDOGCTI_CTRL Register

The SCP_WDOGCTI_CTRL Register characteristics are:

Purpose

CTI trigger mask register.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SCP_WDOGCTI_CTRL Register bit assignments.

Table 104: SCP_WDOGCTI_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:8]	TODBGENSEL	RW	CTI TODBGENSEL input. Reset value 0x00.
[7:0]	-	-	Reserved.

4.5.76 DBGEXPCTI_CTRL Register

The DBGEXPCTI_CTRL Register characteristics are:

Purpose

CTI trigger mask register.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the DBGEXPCTI_CTRL Register bit assignments.

Table 105: DBGEXPCTI_CTRL Register bit assignments

Bits	Name	Type	Function
[31:24]	TODBGENSEL2	RW	CTI2 TODBGENSEL input. Reset value 0x00 .
[23:16]	TINIDENSEL2	RW	CTI2 TINIDENSEL input. Reset value 0x00 .
[15:8]	TODBGENSEL1	RW	CTI1 TODBGENSEL input. Reset value 0x00 .
[7:0]	TINIDENSEL1	RW	CTI1 TINIDENSEL input. Reset value 0x00 .

4.5.77 PCIE_PM_CTRL Register

The PCIE_PM_CTRL Register characteristics are:

Purpose

PCIe power control register.

Usage constraints

Bit[1] is read-only. Bit[0] is read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PCIE_PM_CTRL Register bit assignments.

Table 106: PCIE_PM_CTRL Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1]	PM_ACK	RO	PCIe powerup acknowledgement: 0b0: Not acknowledge. 0b1: Acknowledge. Reset value 0b0.
[0]	PM_REQ	RW	PCIe powerup request: 0b0: No effect. 0b1: Request powerup. Reset value 0b0.

4.5.78 CCIX_PM_CTRL Register

The CCIX_PM_CTRL Register characteristics are:

Purpose

CCIX power control register.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CCIX_PM_CTRL Register bit assignments.

Table 107: CCIX_PM_CTRL Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1]	PM_ACK	RO	CCIX powerup acknowledgement: 0b0: Not acknowledge. 0b1: Acknowledge. Reset value 0b0.
[0]	PM_REQ	RW	CCIX powerup request: 0b0: No effect. 0b1: Request powerup. Reset value 0b0.

4.5.79 SCDBG_CTRL Register

The SCDBG_CTRL Register characteristics are:

Purpose

SCC scan-based debug control register.

Usage constraints

Bits[9:8] and bits[5:4] are read-only. Bits[15:0] are reserved. All other bits are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the SCDBG_CTRL Register bit assignments.

Table 108: SCDBG_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	MANUAL_TRIG_DELAY	RW	<p>Number of REFCLK cycles to wait after a write to MANUAL_TRIGGER register.</p> <p>Default 0x0000.</p> <p>Maximum 0xFFFF.</p> <p>Reset value 0x0000.</p>
[15:10]	-	-	Reserved.
[9]	SOC_ELAOUTUT0	RO	<p>Or-ed SoC ELA EALOUTPUT[0].</p> <p>Reset value 0b0.</p>
[8]	MODE_STATUS	RO	<p>Sticky signal which indicates that the N1 SoC has entered Scan-based debug mode:</p> <p>0b0: Not Scan-based debug mode.</p> <p>0b1: Scan-based debug mode.</p> <p>Reset value 0b0.</p>
[7]	MANUAL_TRIG	RW	<p>Triggers scan-based dump if TRIG_MANUAL is enabled:</p> <p>0b0: No effect.</p> <p>0b1: Trigger scan-based dump.</p> <p>Reset value 0b0.</p>
[6]	TRIG_MANUAL	RW	<p>Include manual trigger:</p> <p>0b0: No effect.</p> <p>0b1: Include manual trigger.</p> <p>Reset value 0b0.</p>
[5]	TRIG_ELA_SOC	RO	<p>Or-ed Logic Analyzer, ELA, STOPCLOCK trigger from all N1 SoC ELAs.</p> <p>Reset value 0b0.</p>

Bits	Name	Type	Function
[4]	TRIG_ELA_AP	RO	Or-ed Logic Analyzer, ELA, STOPCLOCK trigger from both N1clusters. Reset value 0b0.
[3]	TRIG_CTHALT_C1	RW	Include N1 cluster 1 cross trigger halt event, OR function of all PE cross trigger halt events. Reset value 0b0.
[2]	TRIG_CTHALT_C0	RW	Include N1 cluster 0 cross trigger halt event, OR function of all PE cross trigger halt events. Reset value 0b0.
[1]	TRIG_SS_RESETRREQ	RW	Include Manageability Control Processor (MC) and System Control Processor (SCP) subsystem reset request. Reset value 0b0.
[0]	MASTER_EN	RW	Scan-based debug master enable. This bit must be 0b1 to enter SCD mode. 0b0: Not enable. 0b1: Enable. Reset value 0b0.

4.5.80 EXP_IF_CTRL Register

The EXP_IF_CTRL Register characteristics are:

Purpose

Controls certain CCIX and PCIe activity.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the EXP_IF_CTRL Register bit assignments.

Table 109: EXP_IF_CTRL Register bit assignments

Bits	Name	Type	Function
[31:24]	-	-	Reserved.
[23:16]	TSIF_WIN_ADDR	RW	<p>Controls the location of the TSIF 1TB address window inside the Application Processor memory map:</p> <p>0-4TB for single chip system.</p> <p>0-8TB for two chip system.</p> <p>This field should be set before the first transaction from any TSIF masters and should not be changed afterwards.</p> <p>Reset value 0x0000_0000.</p>
[15:2]	-	-	Reserved.
[1]	ROUNDROBIN_TBU_CCIX	RW	<p>Defines the Micro TLB entry replacement policy for the PCIe AXI expansion interface.</p> <p>0b0: The Micro TLB uses a pseudo Least Recently Used (LRU) replacement policy. This policy typically provides the best average performance. However, when multiple translations are prefetched using a StashTranslation transaction, they might evict each other.</p> <p>0b1: The Micro TLB uses a round-robin replacement policy. This policy enables prefetch multiple translations using a StashTranslation transaction without evictions if the Micro TLB size is not exceeded.</p> <p>To avoid evictions, set this bit to 0b1 if a real-time upstream master prefetches translations.</p>

Bits	Name	Type	Function
[0]	ROUNDROBIN_TBU_PCIE	RW	<p>Defines the Micro TLB entry replacement policy for the CCIX AXI expansion interface.</p> <p>0b0: The Micro TLB uses a pseudo Least Recently Used (LRU) replacement policy. This policy typically provides the best average performance. However, when multiple translations are prefetched using a StashTranslation transaction, they might evict each other.</p> <p>0b1: The Micro TLB uses a round-robin replacement policy. This policy enables prefetch multiple translations using a StashTranslation transaction without evictions if the Micro TLB size is not exceeded.</p> <p>To avoid evictions, set this bit to 0b1 if a real-time upstream master prefetches translations.</p>

4.5.81 RO_CTRL Register

The RO_CTRL Register characteristics are:

Purpose

Enables ring oscillator to directly measure silicon liveliness.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the RO_CTRL Register bit assignments.

Table 110: RO_CTRL Register bit assignments

Bits	Name	Type	Function
[31:1]	-	-	Reserved.

Bits	Name	Type	Function
[0]	RO_EN	RW	Enables and disables ring oscillator: 0b0: Disable ring oscillator. 0b1: Enable ring oscillator. Reset value 0b1.

4.5.82 CMN_CCIX_CTRL Register

The CMN_CCIX_CTRL Register characteristics are:

Purpose

CCIX control register.

Usage constraints

Bits[27:2] and bits[19:17] are read-only. Bit[24] and bits[16:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CMN_CCIX_CTRL Register bit assignments.

Table 111: CMN_CCIX_CTRL Register bit assignments

Bits	Name	Type	Function
[31:28]	-	-	Reserved.
[27]	CXLA_CXSCLK_QDENY	RO	QDENY of CXLA CXSCLK control Q channel at CXS interface side. Reset value 0b0.
[26]	CXLA_CXSCLK_QACCEPT	RO	QACCEPTn of CXLA CXSCLK control Q channel at CXS interface side. Reset value 0b0.
[25]	CXLA_CXSCLK_QACTIVE	RO	QACTIVE of CXLA CXSCLK control Q channel at CXS interface side. Reset value 0b0.

Bits	Name	Type	Function
[24]	CXLA_CXSCLK_QREQ	RW	<p>QREQn of CXLA CXSCLK control Q channel at CXS interface side.</p> <p>This bit maintains its reset value while the CCIX subsystem is operating. It is only used to complete Q-channel clock down handshake when the CCIX subsystem, CCIX PCIe controller, needs reset while the main part of CMN-600 is running. This is useful for CCIX subsystem error clearance.</p> <p>Reset value 0b1.</p>
[23:20]	-	-	Reserved.
[19]	CXLA_PWR_QDENY	RO	QDENY of CXLA power control Q channel at CXS interface side.
[18]	CXLA_PWR_QACCEPT	RO	QACCEPTN of CXLA power control Q channel at CXS interface side.
[17]	CXLA_PWR_QACTIVE	RO	QACTIVE of CXLA power control Q channel at CXS interface side.
[16]	CXLA_PWR_QREQ	RW	<p>QREQn of CXLA power control Q channel at CXS interface side.</p> <p>This bit maintains its reset value while the CCIX subsystem is operating. It is only used to complete Q-channel power down handshakes when the CCIX subsystem, CCIX PCIe controller, needs reset while the main part of CMN-600 is running. This is useful for CCIX subsystem error clearance.</p> <p>Reset value 0b1.</p>
[15:0]	PCIE_BUS_NUM	RW	<p>The PCIe ID{BUS_NUM[15:8], DEVICE_NUM[7:3], FUNCTION_NUM[2:0]} used for CMN-600 to form its PCIe header.</p> <p>When the CCIX is configured as RP, this field must be set to 0x0.</p> <p>When the CCIX is configured as EP, the SCP reads the End Point Bus and Device Number Register of CCIX enabled PCIe controller and set the value accordingly.</p> <p>Interrupt ccix_bus_device_change_irq indicates a change of value in the controller.</p>

4.5.83 STM_CTRL Register

The STM_CTRL Register characteristics are:

Purpose

Non-secure guaranteed access control.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the STM_CTRL Register bit assignments.

Table 112: STM_CTRL Register bit assignments

Bits	Name	Type	Function
[31:1]	-	-	Reserved.
[0]	NSGUAREN	RW	<p>The top level static configuration port, NSGUAREN port, NSGUAREN, controls the behavior of the the <i>System Trace Macrocell</i> (STM) for Non-secure guaranteed AXI accesses:</p> <p>0b0: Non-secure guaranteed accesses behave like invariant timing accesses, that is, the AXI does not stall.</p> <p>0b1: Non-secure guaranteed accesses are enabled, that is, the AXI can stall and the trace output is guaranteed.</p> <p>Reset value 0b0.</p>

4.5.84 AXI_OVRD_PCIE Register

The AXI_OVRD_PCIE Register characteristics are:

Purpose

Controls PCIe AXI slave expansion interface override.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the AXI_OVRD_PCIE Register bit assignments.

Table 113: AXI_OVRD_PCIE Register bit assignments

Bits	Name	Type	Function
[31:22]	-	-	Reserved.
[21:20]	AWDOMAIN_TPH	RW	Override value of AWCACHE when TPH values are present. Reset value 0b11.
[19:16]	AWCACHE_TPH	RW	Override value of AWCACHE when TPH values are present. Reset value 0b0000.
[15:14]	-	-	Reserved.
[13:12]	ARDOMAIN	RW	Override value of ARCACHE. Reset value 0b11.
[11:8]	ARCACHE	RW	Override value of AWCACHE. Reset value 0b0000.
[7:6]	-	-	Reserved.
[5:4]	AWDOMAIN	RW	Override value of AWCACHE when TPH values are not present. Reset value 0b11.
[3:0]	AWCACHE	RW	Override value of AWCACHE when TPH values are not present. Reset value 0b0000.

4.5.85 AXI_OVRD_CCIX Register

The AXI_OVRD_CCIX Register characteristics are:

Purpose

Controls CCIX AXI slave expansion interface override.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the AXI_OVRD_CCIX Register bit assignments.

Table 114: AXI_OVRD_CCIX Register bit assignments

Bits	Name	Type	Function
[31:22]	-	-	Reserved.
[21:20]	AWDOMAIN_TPH	RW	Override value of AWCACHE when TPH values are present. Reset value 0b11 .
[19:16]	AWCACHE_TPH	RW	Override value of AWCACHE when TPH values are present. Reset value 0b0000.
[15:14]	-	-	Reserved.
[13:12]	ARDOMAIN	RW	Override value of ARCACHE. Reset value 0b11 .
[11:8]	ARCACHE	RW	Override value of AWCACHE. Reset value 0b0000.
[7:6]	-	-	Reserved.
[5:4]	AWDOMAIN	RW	Override value of AWCACHE when TPH values are not present. Reset value 0b11 .

Bits	Name	Type	Function
[3:0]	AWCACHE	RW	Override value of AWCACHE when TPH values are not present. Reset value 0b0000.

4.5.86 AXI_OVRD_TSIF Register

The AXI_OVRD_TSIF Register characteristics are:

Purpose

Controls TSIF AXI slave expansion interface override.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the AXI_OVRD_TSIF Register bit assignments.

Table 115: AXI_OVRD_CCIX Register bit assignments

Bits	Name	Type	Function
[31:14]	-	-	Reserved.
[13:12]	ARDOMAIN	RW	Override value of ARCACHE. Reset value 0b11 .
[11:6]	-	-	Reserved.
[5:4]	AWDOMAIN	RW	Override value of AWCACHE. Reset value 0b11 .
[3:0]	-	-	Reserved.

4.5.87 GPU_TEXFMTENABLE Register

The GPU_TEXFMTENABLE Register characteristics are:

Purpose

Controls GPU compressed texture format support.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the GPU_TEXFMTENABLE Register bit assignments.

Table 116: GPU_TEXFMTENABLE Register bit assignments

Bits	Name	Type	Function
[31:0]	NORR_TEXFMTENABLE	RW	Norr compressed texture format support.

4.5.88 TRACE_PAD_CTRL0 Register

The TRACE_PAD_CTRL0 Register characteristics are:

Purpose

Controls the drive strengths and slew rates of trace data output pads.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the TRACE_PAD_CTRL0 Register bit assignments.

Table 117: TRACE_PAD_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31:29]	-	-	Reserved.

Bits	Name	Type	Function
[28]	IO_SR_TRACE_DATA 3	RW	Slew rate control of trace port output pads TRACE_DATA[31:24]: 0b0: Fast. 0b1: Slow. Reset value 0b1.
[27:26]	-	-	Reserved.
[25:24]	IO_DS_TRACE_DATA 3	RW	Drive strength control of trace port output pads TRACE_DATA[31:24]: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b01.
[23:21]	-	-	Reserved.
[20]	IO_SR_TRACE_DATA 2	RW	Slew rate control of trace port output pads TRACE_DATA[23:16]: 0b0: Fast. 0b1: Slow. Reset value 0b1.
[19:18]	-	-	Reserved.
[17:16]	IO_DS_TRACE_DATA 2	RW	Drive strength control of trace port output pads TRACE_DATA[23:16]: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b01.

Bits	Name	Type	Function
[15:13]	-	-	Reserved.
[12]	IO_SR_TRACE_DATA 1	RW	Slew rate control of trace port output pads TRACE_DATA[15:8]: 0b0: Fast. 0b1: Slow. Reset value 0b1.
[11:10]	-	-	Reserved.
[9:8]	IO_DS_TRACE_DATA 1	RW	Drive strength control of trace port output pads TRACE_DATA[15:8]: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b01.
[7:5]	-	-	Reserved.
[4]	IO_SR_TRACE_DATA 0	RW	Slew rate control of trace port output pads TRACE_DATA[7:0]: 0b0: Fast. 0b1: Slow. Reset value 0b1.
[3:2]	-	-	Reserved.

Bits	Name	Type	Function
[1:0]	IO_DS_TRACE_DATA 0	RW	Drive strength control of trace port output pads TRACE_DATA[7:0]: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b01.

4.5.89 TRACE_PAD_CTRL1 Register

The TRACE_PAD_CTRL1 Register characteristics are:

Purpose

Controls the drive strengths and slew rates of the trace clock output pads.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the TRACE_PAD_CTRL1 Register bit assignments.

Table 118: TRACE_PAD_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31:13]	-	-	Reserved.
[12]	IO_SR_TRACE_CLK_B	RW	Slew rate control of trace port output pad TRACE_CLK_B: 0b0: Fast. 0b1: Slow. Reset value 0b1.

Bits	Name	Type	Function
[11:10]	-	-	Reserved.
[9:8]	IO_DS_TRACE_CLK_B	RW	Drive strength control of trace port output pad TRACE_CLK_B: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b01 .
[7:5]	-	-	Reserved.
[4]	IO_SR_TRACE_CLK_A	RW	Slew rate control of trace port output pad TRACE_CLK_A: 0b0: Fast. 0b1: Slow. Reset value 0b1.
[3:2]	-	-	Reserved.
[1:0]	IO_DS_TRACE_CLK_A	RW	Drive strength control of trace port output pad TRACE_CLK_A: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b01 .

4.5.90 IOFPGA_TMIF_PAD_CTRL Register

The IOFPGA_TMIF_PAD_CTRL Register characteristics are:

Purpose

Controls the drive strengths and slew rates of IOFPGA AXI TMIF output pads.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the IOFPGA_TMIF_PAD_CTRL Register bit assignments.

Table 119: IOFPGA_TMIF_PAD_CTRL Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20]	IO_SR_IOFPGA_AXI_TMIF_CLK	RW	Slew rate control of IOFPGA AXI TMIF output pad IOFPGA_TMIF_CLK_O: 0b0: Fast. 0b1: Slow. Reset value 0b1.
[19:18]	-	-	Reserved.
[17:16]	IO_DS_IOFPGA_AXI_TMIF_CLK	RW	Drive strength control of IOFPGA AXI TMIF output pad IOFPGA_TMIF_CLK_O: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b01.
[15:13]	-	-	Reserved.
[12]	IO_SR_IOFPGA_AXI_TMIF_CTL	RW	Slew rate control of IOFPGA AXI TMIF output pads IOFPGA_TMIF_VALID_O and IOFPGA_TMIF_CTL_O: 0b0: Fast. 0b1: Slow. Reset value 0b1.

Bits	Name	Type	Function
[11:10]	-	-	Reserved.
[9:8]	IO_DS_IOFPGA_AXI_TMIF_CTL	RW	<p>Drive strength control of IOFPGA AXI TMIF output pads IOFPGA_TMIF_VALID_O and IOFPGA_TMIF_CTL_O:</p> <p>0b00: 2mA.</p> <p>0b01: 8mA.</p> <p>0b10: 4mA.</p> <p>0b11: 12mA.</p> <p>Reset value 0b01.</p>
[7:5]	- -		Reserved.
[4]	IO_SR_IOFPGA_AXI_TMIF_DATA	RW	<p>Slew rate control of IOFPGA AXI TMIF output pads IOFPGA_TMIF_DATA_O[7:0]:</p> <p>0b0: Fast.</p> <p>0b1: Slow.</p> <p>Reset value 0b1.</p>
[3:2]	-	-	Reserved.
[1:0]	IO_DS_IOFPGA_AXI_TMIF_DATA	RW	<p>Drive strength control of IOFPGA AXI TMIF output pads IOFPGA_TMIF_DATA_O[7:0]:</p> <p>0b00: 2mA.</p> <p>0b01: 8mA.</p> <p>0b10: 4mA.</p> <p>0b11: 12mA.</p> <p>Reset value 0b01.</p>

4.5.91 IOFPGA_TSIF_PAD_CTRL Register

The IOFPGA_TSIF_PAD_CTRL Register characteristics are:

Purpose

Controls the drive strengths and slew rates of IOFPGA AXI TSIF output pads.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the IOFPGA_TSIF_PAD_CTRL Register bit assignments.

Table 120: IOFPGA_TSIF_PAD_CTRL Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20]	IO_SR_IOFPGA_AXI_TSIF_CLK	RW	Slew rate control of IOFPGA AXI TSIF output pad IOFPGA_TSIF_CLK_O: 0b0: Fast. 0b1: Slow. Reset value 0b1.
[19:18]	-	-	Reserved.
[17:16]	IO_DS_IOFPGA_AXI_TSIF_CLK	RW	Drive strength control of IOFPGA AXI TSIF output pad IOFPGA_TSIF_CLK_O: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b01.
[15:13]	-	-	Reserved.

Bits	Name	Type	Function
[12]	IO_SR_IOFPGA_AXI_TSIF_CTL	RW	<p>Slew rate control of IOFPGA AXI TSIF output pads IOFPGA_TSIF_VALID_O and IOFPGA_TSIF_CTL_O[1:0]:</p> <p>0b0: Fast.</p> <p>0b1: Slow.</p> <p>Reset value 0b1.</p>
[11:10]	-	-	Reserved.
[9:8]	IO_DS_IOFPGA_AXI_TSIF_CTL	RW	<p>Drive strength control of IOFPGA AXI TSIF output pads IOFPGA_TSIF_VALID_O and IOFPGA_TSIF_CTL_O[1:0]:</p> <p>0b00: 2mA.</p> <p>0b01: 8mA.</p> <p>0b10: 4mA.</p> <p>0b11: 12mA.</p> <p>Reset value 0b01.</p>
[7:5]	-	-	Reserved.
[4]	IO_SR_IOFPGA_AXI_TSIF_DATA	RW	<p>Slew rate control of IOFPGA AXI TSIF output pads IOFPGA_TSIF_DATA_O[7:0]:</p> <p>0b0: Fast.</p> <p>0b1: Slow.</p> <p>Reset value 0b1.</p>
[3:2]	-	-	Reserved.

Bits	Name	Type	Function
[1:0]	IO_DS_IOFPGA_AXI_TSIF_DATA	RW	Drive strength control of IOFPGA AXI TSIF output pads IOFPGA_TSIF_DATA_O[7:0]: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b01.

4.5.92 DISPLAY_PAD_CTRL0 Register

The DISPLAY_PAD_CTRL0 Register characteristics are:

Purpose

Controls the drive strengths and slew rates of the DPU output pads.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the DISPLAY_PAD_CTRL0 Register bit assignments.

Table 121: DISPLAY_PAD_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31:29]	-	-	Reserved.
[28]	IO_SR_DATAEN	RW	Slew rate control of display output pad DATAEN: 0b0: Fast. 0b1: Slow. Reset value 0b0.
[27:26]	-	-	Reserved.

Bits	Name	Type	Function
[25:24]	IO_DS_DATAEN	RW	Drive strength control of display output pad DATAEN: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b1.
[23:21]	-	-	Reserved.
[20]	IO_SR_VSYNC	RW	Slew rate control of display output pad VSYNC: 0b0: Fast. 0b1: Slow. Reset value 0b0.
[19:18]	-	-	Reserved.
[17:16]	IO_DS_VSYNC	RW	Drive strength control of display output pad VSYNC: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b1.
[15:13]	-	-	Reserved.
[12]	IO_SR_HSYNC	RW	Slew rate control of display output pad HSYNC: 0b0: Fast. 0b1: Slow. Reset value 0b0.
[11:10]	-	-	Reserved.

Bits	Name	Type	Function
[9:8]	IO_DS_HSYNC	RW	Drive strength control of display output pad HSYNC: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b1.
[7:5]	-	-	Reserved.
[4]	IO_SR_PXLCLK	RW	Slew rate control of display output pad PXLCLK: 0b0: Fast. 0b1: Slow. Reset value 0b0.
[3:2]	-	-	Reserved.
[1:0]	IO_DS_PXLCLK	RW	Drive strength control of display output pad PXLCLK: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b1.

4.5.93 DISPLAY_PAD_CTRL1 Register

The DISPLAY_PAD_CTRL1 Register characteristics are:

Purpose

Controls the drive strengths and slew rates of the DPU output pads.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the DISPLAY_PAD_CTRL1 Register bit assignments.

Table 122: DISPLAY_PAD_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20]	IO_SR_PXLDATAB	RW	<p>Slew rate control of display output pads PXLDATAB_0 ~ PXLDATAB_7:</p> <p>0b0: Fast.</p> <p>0b1: Slow.</p> <p>Reset value 0b0.</p>
[19:18]	-	-	Reserved.
[17:16]	IO_DS_PXLDATAB	RW	<p>Drive strength control of display output pads PXLDATAB_0 ~ PXLDATAB_7:</p> <p>0b00: 2mA.</p> <p>0b01: 8mA.</p> <p>0b10: 4mA.</p> <p>0b11: 12mA.</p> <p>Reset value 0b1.</p>
[15:13]	-	-	Reserved.
[12]	IO_SR_PXLDTAG	RW	<p>Slew rate control of display output pads PXLDTAG_0 ~ PXLDTAG_7:</p> <p>0b0: Fast.</p> <p>0b1: Slow.</p> <p>Reset value 0b0.</p>
[11:10]	-	-	Reserved.

Bits	Name	Type	Function
[9:8]	IO_DS_PXLDATAG	RW	Drive strength control of display output pads PXLDATAG_0 ~ PXLDATAG_7: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b1.
[7:5]	-	-	Reserved.
[4]	IO_SR_PXLDATAR	RW	Slew rate control of display output pads PXLDATAR_0 ~ PXLDATAR_7: 0b0: Fast. 0b1: Slow. Reset value 0b0.
[3:2]	-	-	Reserved.
[1:0]	IO_DS_PXLDATAR	RW	Drive strength control of display output pads PXLDATAR_0 ~ PXLDATAR_7: 0b00: 2mA. 0b01: 8mA. 0b10: 4mA. 0b11: 12mA. Reset value 0b1.

4.5.94 APB_CTRL_CLR Register

The APB_CTRL_CLR Register characteristics are:

Purpose

Controls reversion to serial control of the register at the specified base address.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the APB_CTRL_CLR Register bit assignments.

Table 123: APB_CTRL_CLR Register bit assignments

Bits	Name	Type	Function
[31:12]	NUMBER	RW	Writing A50F5 to this field sets the register, whose base address bits[11:0] specify, to serial control.
[11:0]	BASE_ADDRESS	RW	Base address of register which reverts to serial control when A50F5 is written to bits[31:12].

4.5.95 PID4 Register

The PID4 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PID4 Register bit assignments.

Table 124: PID4 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PID4	RO	Peripheral ID 4 identification. Reset value 0x04 .

4.5.96 PID0 Register

The PID0 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PID0 Register bit assignments.

Table 125: PID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PID0	RO	Peripheral ID 0 identification. Reset value 0xA7.

4.5.97 PID1 Register

The PID1 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PID1 Register bit assignments.

Table 126: PID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PID1	RO	Peripheral ID 1 identification. Reset value 0xB0 .

4.5.98 PID2 Register

The PID2 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PID2 Register bit assignments.

Table 127: PID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PID2	RO	Peripheral ID 2 identification. Reset value 0x0B .

4.5.99 PID3 Register

The PID3 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the PID3 Register bit assignments.

Table 128: PID3 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PID3	RO	Peripheral ID 3 identification. Reset value 0x00 .

4.5.100 CID0 Register

The CID0 Register characteristics are:

Purpose

Stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CID0 Register bit assignments.

Table 129: CID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	CID3	RO	Component ID 3 identification. Reset value 0x0D .

4.5.101 CID1 Register

The CID1 Register characteristics are:

Purpose

Stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CID1 Register bit assignments.

Table 130: CID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	CID1	RO	Component ID 1 identification. Reset value 0xF0 .

4.5.102 CID2 Register

The CID2 Register characteristics are:

Purpose

Stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CID2 Register bit assignments.

Table 131: CID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	CID2	RO	Component ID 2 identification. Reset value 0x05 .

4.5.103 CID3 Register

The CID3 Register characteristics are:

Purpose

Stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [System Configuration Control registers summary](#).

The following table shows the CID3 Register bit assignments.

Table 132: CID3 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	CID3	RO	Component ID 3 identification. Reset value 0xB1 .

4.6 APB system registers

The IOFPGA contains the APB system registers.

4.6.1 APB system register summary

The base memory address of the APB system registers in the IOFPGA is 0x1C01_0000.

The following table shows the registers in address offset order from the base memory address.

Base memory address

0x1C01_0000

Table 133: N1 SDP APB system register summary

Offset	Name	Type	Reset	Width	Description
0x0000	SYS_ID	RO	0XXXXXXXXX	32	See SYS_ID Register.
0x0004	SYS_SW	RO/RW	0X000000XX	32	See SYS_SW Register.
0x0008	SYS_LED	RO/RW	0x000000XX	32	See SYS_LED Register.
0x0024	SYS_100HZ	RO/RW	0XXXXXXXXX	32	See SYS_100HZ Register.
0x0030	SYS_FLAG	RO	0x00000000	32	See SYS_FLAG Registers.
0x0030	SYS_FLAGSSET	WO	-	32	See SYS_FLAG Registers.
0x0034	SYS_FLAGSCLR	WO	-	32	See SYS_FLAG Registers.
0x0038	SYS_NVFLAGS	RO	0x00000000	32	See SYS_FLAG Registers.
0x0038	SYS_NVFLAGSSET	WO	-	32	See SYS_FLAG Registers.
0x003C	SYS_NVFLAGSCLR	WO	-	32	See SYS_FLAG Registers.
0x0058	SYS_CFGSW	RO/RW	0x000000XX	32	See SYS_CFGSW Register.
0x005C	SYS_24MHZ	RO	0XXXXXXXXX	32	See SYS_24MHZ Register.
0x0070	SYS_PCIE_CNTL	RW	0x0000000X	32	See SYS_PCIE_CNTL Register.
0x0074	SYS_PCIE_GBE_L	RO	0XXXXXXXXX	32	See SYS_PCIE_GBE Register.
0x0078	SYS_PCIE_GBE_H	RO	0x0000XXXX	32	See SYS_PCIE_GBE Register.
0x0084	SYS_PROC_ID0	RW	0x0X000000	32	See SYS_PROC_ID0 Register.

Offset	Name	Type	Reset	Width	Description
0x0120	SYS_FAN_SPEED	RW	0x00000000	32	See SYS_FAN_SPEED Register .

4.6.2 SYS_ID Register

The SYS_ID Register characteristics are:

Purpose

Contains information about the Morello SDP and the bus and image versions inside the IOFPGA.

Usage constraints

The SYS_ID Register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 134: SYS_ID Register bit assignments

Bits	Name	Type	Function
[31:28]	Rev	RO	Board revision: 0x0: Rev A board. This is the prototype board and contains the Morello SoC.
[26:16]	HBI	RO	HBI board number in BCD: 0x316: HBI0316.
[15:12]	Build	RO	Build variant of board: 0xF: All builds.
[11:8]	Arch	RO	IOFPGA bus architecture: 0x4: AHB. 0x5: AXI.

Bits	Name	Type	Function
[7:0]	FPGA	RO	FPGA build in BCD. The actual value that is read depends on the FPGA build.

4.6.3 SYS_SW Register

The SYS_SW Register characteristics are:

Purpose

Stores the 8 user DIP switches on the Morello board. A bit set to 1 indicates that the switch is ON.

Usage constraints

Bits[29:28] are read-only. Bits[7:0] are read/write.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 135: SYS_SW Register bit assignments

Bits	Name	Type	Function
[31:30]	-	-	Reserved.
[29]	nUARTOCTS	RO	UART0 CTS signal.
[28]	nUARTODSR	RO	UART0 DSR signal.
[27:8]	-	-	Reserved.
[7:0]	HARD_WARE_USER_SW.	RW	State of the 8 user DIP switches on the board. Application software can read these switch settings: 0b0: OFF. 0b1: ON.

4.6.4 SYS_LED Register

The SYS_LED Register characteristics are:

Purpose

Controls the eight user LEDs on the Morello board. All LEDs are turned OFF at reset. The Boot Monitor updates the LED value.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 136: SYS_LED Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	LED[7:0]	RW	Set or read the user LED states: 0b0: OFF. 0b1: ON.

4.6.5 SYS_100HZ Register

The SYS_100HZ Register characteristics are:

Purpose

A 32-bit counter that updates at 100Hz. The input clock derives from the 24MHz clock generator on the Morello board.

Usage constraints

The SYS_100HZ Register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 137: SYS_100HZ Register bit assignments

Bits	Name	Type	Function
[31:0]	100HZ_COUNT	RO	Contains the count, at 100Hz, since the last CB_nRST reset.

4.6.6 SYS_FLAG Registers

The SYS_FLAG Registers characteristics are:

Purpose

Provide two 32-bit registers, SYS_FLAGS and SYS_NVFLAGS, that contain general-purpose flags. The application software defines the meaning of the flags. You use the SYS_FLAGSSET, SYS_FLAGSCLR, SYS_NVFLAGSSET, and SYS_NVFLAGSCLR registers to set and clear the bits in the Flag Registers.

Usage constraints

The SYS_FLAGS and SYS_NVFLAGS Registers are read-only.

The SYS_FLAGSSET, SYS_FLAGSCLR, SYS_NVFLAGSSET, and SYS_NVFLAGSCLR Registers are write-only.

Configurations

Available in all Morello SDP configurations.

SYS_FLAGS Register

The SYS_FLAGS Register is one of the two flag registers. It contains the current states of the flags.

The SYS_FLAGS Register is volatile, that is, a reset signal from the reset push button resets the SYS_FLAGS Register.

You use the SYS_FLAGSSET Register to set bits in the SYS_FLAGS Register. Write 1 to set the associated flag. Write 0 to leave the associated flag unchanged.

You use the SYS_FLAGSCLR Register to clear bits in the SYS_FLAGS Register. Write 1 to clear the associated flag. Write 0 to leave the associated flag unchanged.

SYS_NVFLAGS Register

The SYS_NVFLAGS Register is one of the two flag registers. It contains the current states of the flags.

The SYS_NVFLAGS Register is non-volatile, that is, a reset signal from the reset push button does not reset the SYS_FLAGS Register. Only **CB_nPOR** resets the SYS_NVFLAGS Register.

You use the SYS_NVFLAGSSET Register to set bits in the SYS_NVFLAGS Register. Write 1 to set the associated flag. Write 0 to leave the associated flag unchanged.

You use the SYS_NVFLAGSCLR Register to clear bits in the SYS_NVFLAGS Register. Write 1 to clear the associated flag. Write 0 to leave the associated flag unchanged.

4.6.7 SYS_CFGSW Register

The SYS_CFGSW Register characteristics are:

Purpose

Contains the value of *CONFSWITCH* in the `config.txt` file.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 138: SYS_CFGSW Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	SOFT_CONFIG_SWITCH	RW	<p>Software applications can read these switch settings. The application software defines the meanings of the switch settings. The reset signals set these bits to the value of <i>CONFSWITCH</i> in the <code>config.txt</code> file.</p> <p>Note: The configuration system does not use the contents of this register for board configuration.</p>

4.6.8 SYS_24MHZ Register

The SYS_24MHZ Register characteristics are:

Purpose

A 32-bit counter that updates at 24MHz. The clock source is the 24MHz clock generator on the Morello SDP.

Usage constraints

This register is read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 139: SYS_24MHZ Register bit assignments

Bits	Name	Type	Function
[31:0]	24MHZ_COUNT	RO	Contains the count, at 24MHz, since the last CB_nRST reset. CB_nRST sets the register to zero and then the count resumes.

4.6.9 SYS_PCIE_CNTL Register

The SYS_PCIE_CNTL Register characteristics are:

Purpose

Error signal from PCIe switch and reset signal to PCIe Express slots.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 140: SYS_PCIE_CNTL Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1]	PCIE_RSTHALT	RW	Error signal from PCIe switch.
[0]	PCIE_nPERST	RW	Reset signal to PCIe expansion slots.

4.6.10 SYS_PCIE_GBE Register

The SYS_PCIE_GBE Register characteristics are:

Purpose

Contains the 48-bit PCI Express Ethernet MAC address.

Usage constraints

Bits[47:0] are read-only.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 141: SYS_PCIE_GBE Register bit assignments

Bits	Name	Type	Function
[63:48]	-	-	Reserved.
[47:32]	SYS_PCIE_GBE_H	RO	Most significant 16 bits of the PCI Express Ethernet MAC address.
[31:0]	SYS_PCIE_GBE_L	RO	Least significant 32 bits of the PCI Express Ethernet MAC address.

4.6.11 SYS_PROC_ID0 Register

The SYS_PROC_ID0 Register characteristics are:

Purpose

Identifies the active clusters in the Morello SoC.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 142: SYS_PROC_ID0 Register bit assignments

Bits	Name	Type	Function
[31:24]	PROC_ID0	RW	Denotes active clusters.
[23:0]	-	-	Reserved.

4.6.12 SYS_FAN_SPEED Register

The SYS_FAN_SPEED Register characteristics are:

Purpose

Contains a value that represents the fan operating speed. The MCC uses this value to moderate the speed of the cooling fan on the Morello SDP.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 143: SYS_FAN_SPEED Register bit assignments

Bits	Name	Type	Function
[31]	UPD ATE_FAN_SPEED	RW	Set this bit to 1 when updating the fan speed control bits [4:0]. The system clears this bit to 0 after updating the fan speed. The default value is 0b0.
[30:5]	-	-	Reserved.

Bits	Name	Type	Function
[4:0]	FAN_SPEED	RW	<p>Indicates and controls the speed of the board cooling fan. The fan has 30 speed settings:</p> <p>0b00010: Minimum fan speed.</p> <p>0b11111: Maximum fan speed.</p> <p>Note: 0b00000 and 0b00001 are invalid settings. Do not use them.</p>

4.6.13 SP810_CTRL Register

The SP810_CTRL Register characteristics are:

Purpose

This register in the SP810 system controller selects the source clocks for the four SP804 timers in the IOFPGA.

Usage constraints

There are no usage constraints.

Configurations

Available in all Morello board configurations.

Memory offset and full register reset value

See [APB system register summary](#).

The following table shows the bit assignments.

Table 144: SP810_CTRL Register bit assignments

Bits	Name	Type	Function
[31:22]	-		Reserved.
[21]	TimerEn3Sel		<p>Selects the source clock for SP804 3 timer clock TIM_CLK[3]:</p> <p>0b0 : TIM_CLK[3] = 32kHz.</p> <p>0b1 : TIM_CLK[3] = 1MHz.</p> <p>Note: The default is 0b0.</p>
[20]	-		Reserved.

Bits	Name	Type	Function
[19]	TimerEn2Sel		Selects the source clock for SP804 2 timer clock TIM_CLK[2]: 0b0 : TIM_CLK[2] = 32kHz. 0b1 : TIM_CLK[2] = 1MHz. Note: The default is 0b0.
[18]	-		Reserved.
[17]	TimerEn1Sel		Selects the source clock for SP804 1 timer clock TIM_CLK[1]: 0b0 : TIM_CLK[1] = 32kHz. 0b1 : TIM_CLK[1] = 1MHz. Note: The default is 0b0.
[16]	-		Reserved.
[15]	TimerEn0Sel		Selects the source clock for SP804 0 timer clock TIM_CLK[0]: 0b0 : TIM_CLK[0] = 32kHz. 0b1 : TIM_CLK[0] = 1MHz. Note: The default is 0b0.
[14:0]	-		Reserved.

4.7 Display clock and power control logic registers

Morello contains the following display clock and power control logic registers.

4.7.1 Display clock and power control logic registers summary

The base memory address of the display clock and power control logic registers in Morello is 0x5062_0000, in the Element management peripherals region of the SCP memory map.

The following table shows the display clock and power control logic registers in offset order from the base memory address. Undefined registers are reserved. Software must not attempt to access these registers.

Base memory address

0x5062_0000

Table 145: Display clock and power control logic registers summary

Offset	Name	Type	Reset	Width	Description
0x000-0x82C	-	RAZ/WI	-	-	Reserved.
0x830	DISPLAYCLK_CTRL	RW	0x0000_0001	32	See DISPLAYCLK_CTRL Register .
0x834	DISPLAYCLK_DIV1	RW/RO	0x0000_001F	32	See DISPLAYCLK_DIV1 Register .
0x838	DISPLAYCLK_DIV2	RW/RO	0x0000_001F	32	See DISPLAYCLK_DIV2 Register . Control register
0x83C-0x9FC	-	RAZ/WI	-	-	Reserved.
0xA00	CLKFORCE_STATUS	RO	-	32	See CLKFORCE_STATUS Register .
0xA04	CLKFORCE_SET	WO	-	32	See CLKFORCE_SET Register .
0xA08	CLKFORCE_CLR	WO	0x0	32	See CLKFORCE_CLR Register .
0xA0C-0xFBC	-	RAZ/WI	-	-	Reserved.
0xFC0	PIK_POWER_CONTROL_LOGIC	RO	0x0052_0001	32	See PIK_POWER_CONTROL_LOGIC Register .
0xFD0	PID4	RO	0x44	8	See PID4 Register .
0xFD4	-	RAZ/WI	-	-	Reserved.
0xFD8	-	RAZ/WI	-	-	Reserved.
0xFDC	-	RAZ/WI	-	-	Reserved.
0xFE0	PID0	RO	0xB8	8	See PID0 Register .
0xFE4	PID1	RO	0xB0	8	See PID1 Register .
0xFE8	PID2	RO	0x0B	8	See PID2 Register .
0xFEC	PID3	RO	0x00	8	See PID3 Register .

Offset	Name	Type	Reset	Width	Description
0xFF0	ID0	RO	0x0D	8	See Component ID0 Register .
0xFF4	ID1	RO	0xF0	8	See Component ID1 Register .
0xFF8	ID2	RO	0x05	8	See Component ID2 Register .
0xFFC	ID3	RO	0xB1	8	See Component ID3 Register .
0x1000 - 0x1FFC	DPU-PPU0	-	-	-	PPU Configuration dependent registers. For the DPU-PPU0 register descriptions, see <i>Arm® Power Policy Unit Architecture Specification</i> .

4.7.2 DISPLAYCLK_CTRL Register

The DISPLAYCLK_CTRL Register characteristics are:

Purpose

Controls the display clock register.

Usage constraints

This register is read-write.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the DISPLAYCLK_CTRL Register bit assignments.

Table 146: DISPLAYCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:24]	ENTRY_DLY	RW	Number of clock cycles between the clock not being required and the request to dynamically clock gate it: 0x0 - No cycles 0x1 - 1 cycle ... 0xFF - 255 cycles
[23:16]	-	-	Reserved.
[15:8]	CLKSELECT_CUR	RO	Acknowledges the currently selected clock source: 0x00 - Clock Gated 0x01 - REFCLK 0x02 - DISPLAYPLLCLK 0x04 - SYSPLLCLK Other values are Reserved.
[7:0]	CLKSELECT	RW	Selects the clock source: 0x00 - Clock Gated 0x01 - REFCLK 0x02 - DISPLAYPLLCLK 0x04 - SYSPLLCLK Other values are Reserved. The result of writing one of the Reserved values into this field is UNPREDICTABLE.

4.7.3 DISPLAYCLK_DIV1 Register

The DISPLAYCLK_DIV1 Register characteristics are:

Purpose

Controls the display clock divider 1 register.

Usage constraints

This register is read-write and read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the DISPLAYCLK_DIV1 Register bit assignments.

Table 147: DISPLAYCLK_DIV1 Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Acknowledges the currently selected clock divider value for the clock source selected by bit n. For example, *CLK_DIV1 acknowledges the divider value for the clock selected when CLKSELECT is 0x02. Currently selected clock divider value for the clock source selected by register DISPLAYCLK_CTRL. Clock divider value = CLKDIV_CUR + 1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Clock divider value for the clock source selected by register DISPLAYCLK_CTR. Clock divider value = CLKDIV + 1.

4.7.4 DISPLAYCLK_DIV2 Register

The DISPLAYCLK_DIV2 Register characteristics are:

Purpose

Controls the display clock divider 2 register.

Usage constraints

This register is read-write and read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the DISPLAYCLK_DIV2 Register bit assignments.

Table 148: DISPLAYCLK_DIV2 Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	<p>Acknowledges the currently selected clock divider value for the clock source selected by bit n. For example, *CLK_DIV2 acknowledges the divider value for the clock selected when CLKSELECT is 0x02.</p> <p>Currently selected clock divider value for the clock source selected by register DISPLAYCLK_CTRL.</p> <p>Clock divider value = CLKDIV_CUR + 1.</p>
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	<p>Clock divider value for the clock source selected by register DISPLAYCLK_CTR.</p> <p>Clock divider value = CLKDIV + 1.</p>

4.7.5 CLKFORCE_STATUS Register

The bit allocation is the same as the CLKFORCE_SET register. If a bit reads as 1 then the associated dynamic clock gating is disabled, otherwise it is enabled. The CLKFORCE_STATUS Register characteristics are:

Purpose

Clock force status register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the CLKFORCE_STATUS Register bit assignments.

Table 149: CLKFORCE_STATUS Register bit assignments

Bits	Name	Type	Function
[31:4]	-	-	Reserved.
[3]	ACLKDPFORCE_STATUS	RO	Clock status for ACLKDP.
[2:0]	-	-	Reserved.

4.7.6 CLKFORCE_SET Register

Writing 1 to a bit within the CLKFORCE_SET register disables any dynamic hardware clock gating, while writing 0 to a bit is ignored. The CLKFORCE_SET Register characteristics are:

Purpose

Clock force set register.

Usage constraints

This register is write-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the CLKFORCE_SET Register bit assignments.

Table 150: CLKFORCE_SET Register bit assignments

Bits	Name	Type	Function
[31:4]	-	-	Reserved.
[3]	ACLKDPFORCE_SET	WO	Write 0b1 to enable clock force.
[2:0]	-	-	Reserved.

4.7.7 CLKFORCE_CLR Register

The bit allocation is the same as the CLKFORCE_SET register. Writing 1 to a bit within the CLKFORCE_CLR register enables the dynamic hardware clocking gating, while writing 0 to a bit is ignored. The CLKFORCE_CLR Register characteristics are:

Purpose

Clock force clear register.

Usage constraints

This register is write-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the CLKFORCE_CLR Register bit assignments.

Table 151: CLKFORCE_CLR Register bit assignments

Bits	Name	Type	Function
[31:4]	-	-	Reserved.
[3]	ACLKDPFORCE_CLR	WO	Write 0b1 to clear (disable) clock force.

Bits	Name	Type	Function
[2:0]	-	-	Reserved.

4.7.8 PIK_POWER_CONTROL_LOGIC Register

The PIK_POWER_CONTROL_LOGIC configuration register characteristics are:

Purpose

Power control logic configuration register. The value is dependent upon chosen configuration.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the PIK_POWER_CONTROL_LOGIC Register bit assignments.

Table 152: PIK_POWER_CONTROL_LOGIC Register bit assignments

Bits	Name	Type	Function
[31:16]	-	RO	POWER CONTROL LOGIC_ID. It is set to 0x0052.
[15:4]	-	-	Reserved
[3:0]	no_of_ppu	RO	Defines the number of PPU's in the POWER CONTROL LOGIC. This value is set to 0x1 to indicate one PPU.

4.7.9 PID4 Register

The PID4 register characteristics are:

Purpose

Peripheral ID 4 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the PID4 Register bit assignments.

Table 153: PID4 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ.
[7:4]	4KB_count	RO	The number of 4KB address blocks required to access the registers, expressed in powers of 2. These bits read back as 0x4. This means that the POWER CONTROL LOGIC occupies 64KB address block.
[3:0]	jep106_c_code	RO	The JEP106 continuation code value represents how many 0x7F continuation characters occur in the identity code of the manufacturer. These bits read back as 0x4.

4.7.10 PID0 Register

The PID0 register characteristics are:

Purpose

Peripheral ID 0 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the PID0 Register bit assignments.

Table 154: PID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ.
[7:0]	part_number_0	RO	These bits read back as 0xB8.

4.7.11 PID1 Register

The PID1 register characteristics are:

Purpose

Peripheral ID 1 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the PID1 Register bit assignments.

Table 155: PID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:4]	jep106_id_3_0	RO	JEP106 identity code [3:0]. See the <i>JEDEC Standard Manufacturer's Identification Code</i> .
[3:0]	part_number_1	RO	These bits read back as 0x0.

4.7.12 PID2 Register

The PID2 register characteristics are:

Purpose

Peripheral ID 2 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the PID2 Register bit assignments.

Table 156: PID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:4]	Revision	RO	Identifies the revision of the base POWER CONTROL LOGIC. For revision r0p0, this field is set to 0x0.
[3]	jedec_used	RO	This indicates that the POWER CONTROL LOGIC uses a <i>manufacturer's identity code</i> that was allocated by JEDEC according to JEP106. This bit always reads back as 0x1.

Bits	Name	Type	Function
[2:0]	jep106_id_6_4	RO	JEP106 identity code [6:4].

4.7.13 PID3 Register

The PID3 register characteristics are:

Purpose

Peripheral ID 3 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the PID3 Register bit assignments.

Table 157: PID3 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:4]	RevAnd	RO	The top-level RTL provides a 4-bit input, ECOREVNUM, that is normally tied LOW and provides a read value of 0x0. When silicon is available, and if metal fixes are necessary, the manufacturer can modify the tie-offs to indicate a revision of the silicon.
[3:0]	mod_number	RO	This is set to 0x0.

4.7.14 Component ID0 Register

The ID0 register characteristics are:

Purpose

Component ID 0 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the Component ID0 Register bit assignments.

Table 158: Component ID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:0]	comp_id_0	RO	These bits read back as 0x0D.

4.7.15 Component ID1 Register

The ID1 register characteristics are:

Purpose

Component ID 1 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the Component ID1 Register bit assignments.

Table 159: Component ID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:0]	comp_id_1	RO	These bits read back as 0xF0.

4.7.16 Component ID2 Register

The ID2 register characteristics are:

Purpose

Component ID 2 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the Component ID2 Register bit assignments.

Table 160: Component ID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:0]	comp_id_2	RO	These bits read back as 0x05.

4.7.17 Component ID3 Register

The ID3 register characteristics are:

Purpose

Component ID 3 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Display clock and power control logic registers summary](#).

The following table shows the Component ID3 Register bit assignments.

Table 161: Component ID3 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:0]	comp_id_2	RO	These bits read back as 0xB1.

4.8 GPU clock and power control logic registers

Morello contains the following GPU clock and power control logic registers.

4.8.1 GPU clock and power control logic registers summary

The base memory address of the GPU clock and power control logic registers in Morello is 0x5063_0000, in the Element management peripherals region of the SCP memory map.

The following table shows the GPU clock and power control logic registers in offset order from the base memory address. Undefined registers are reserved. Software must not attempt to access these registers.

Base memory address

0x5063_0000

Table 162: GPU clock and power control logic registers summary

Offset	Name	Type	Reset	Width	Description
0x000-0x7FC	-	RAZ/WI	-	-	Reserved.
0x800-0x80C	-	RAZ/WI	-	-	Reserved.
0x810	GPUCLK_CTRL	RW	0x0000_0001	32	See GPUCLK_CTRL Register .
0x814	GPUCLK_DIV1	RW	0x0000_001F	32	See GPUCLK_DIV1 Register .
0x818	GPUCLK_DIV2	RW	0x0000_001F	32	See GPUCLK_DIV2 Register .
0x81C	-	RAZ/WI	-	-	Reserved.
0x820	ACLKGPU_CTRL	RW	0x0000_00F0	32	See ACLKGPU_CTRL Register .
0x824-0x9FC	-	RAZ/WI	-	-	Reserved.
0xA00	CLKFORCE_STATUS	RO	-	32	See CLKFORCE_STATUS Register .
0xA04	CLKFORCE_SET	WO	-	32	See CLKFORCE_SET Register .
0xA08	CLKFORCE_CLR	WO	0x0	32	See CLKFORCE_CLR Register .
0xA0C-0xFB8	-	RAZ/WI	0x0	-	Reserved.

Offset	Name	Type	Reset	Width	Description
0xFBC	CAP	RO	-	32	See CAP Register .
0xFC0	PIK_POWER_CONTROL_LOGIC	RO	0x0041_0001	32	See PIK_POWER_CONTROL_LOGIC Register .
0xFD0	PID4	RO	0x44	8	See PID4 Register .
0xFD4	-	RAZ/WI	-	-	Reserved.
0xFD8	-	RAZ/WI	-	-	Reserved.
0xFDC	-	RAZ/WI	-	-	Reserved.
0xFE0	PID0	RO	0xB8	8	See PID0 Register .
0xFE4	PID1	RO	0xB0	8	See PID1 Register .
0xFE8	PID2	RO	0x0B	8	See PID2 Register .
0xFEC	PID3	RO	0x00	8	See PID3 Register .
0xFF0	ID0	RO	0x0D	8	See Component ID0 Register .
0xFF4	ID1	RO	0xF0	8	See Component ID1 Register .
0xFF8	ID2	RO	0x05	8	See Component ID2 Register .
0xFFC	ID3	RO	0xB1	8	See Component ID3 Register .
0x1000 - 0x1FFC	GPU-PPU0	-	-	-	PPU Configuration dependent registers. For the DPU-PPU0 register descriptions, see Arm® Power Policy Unit Architecture Specification .

4.8.2 GPUCLK_CTRL Register

The GPUCLK_CTRL Register characteristics are:

Purpose

Controls the GPU Clock Control register.

Usage constraints

This register is read-write.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the GPUCLK_CTRL Register bit assignments.

Table 163: GPUCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:24]	ENTRY_DLY	RW	<p>Number of clock cycles between the clock not being required and the request to dynamically clock gate it:</p> <p>0x0 - No cycles</p> <p>0x1 - 1 cycle</p> <p>...</p> <p>0xFF - 255 cycles</p> <p>This field is only available if CAP register bit 0 is set to a 1. Otherwise it is Reserved.</p>
[23:16]	-	-	Reserved.
[15:8]	CLKSELECT_CUR	RO	<p>Acknowledges the currently selected clock source:</p> <p>0x00 - Clock Gated</p> <p>0x01 - REFCLK</p> <p>0x02 - SYSPLLCLK</p> <p>0x04 - GPUPLLCLK</p> <p>Other values are Reserved.</p>

Bits	Name	Type	Function
[7:0]	CLKSELECT	RW	<p>Selects the clock source:</p> <p>0x00 - Clock Gated</p> <p>0x01 - REFCLK</p> <p>0x02 - SYSPLLCLK</p> <p>0x04 - GUPPLLCLK</p> <p>Other values are Reserved. The result of writing one of the Reserved values into this field is UNPREDICTABLE.</p>

4.8.3 GPUCLK_DIV1 Register

The GPUCLK_DIV1 Register characteristics are:

Purpose

Controls the GPU clock divider control 1 register.

Usage constraints

This register is read-write and read only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the GPUCLK_DIV1 Register bit assignments.

Table 164: GPUCLK_DIV1 Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.

Bits	Name	Type	Function
[20:16]	CLKDIV_CUR	RO	<p>Acknowledges the currently selected clock divider value for the clock source selected by bit n. For example, GPUCLK_DIV1 acknowledges the divider value for the clock selected when CLKSELECT is 0x02.</p> <p>Currently selected clock divider value for the clock source selected by register GPUCLK_CTRL.</p> <p>Clock divider value = CLKDIV_CUR + 1.</p>
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	<p>GPUCLK_DIVn register requests a new clock divider value for the clock source selected by bit n. For example, GPUCLK_DIV1 selects the divider value for the clock selected when CLKSELECT is 0x02.</p> <p>Clock divider value = CLKDIV + 1.</p>

4.8.4 GPUCLK_DIV2 Register

The GPUCLK_DIV2 Register characteristics are:

Purpose

Controls the GPU clock divider control 2 register.

Usage constraints

This register is read-write and read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the GPUCLK_DIV2 Register bit assignments.

Table 165: GPUCLK_DIV2 Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	<p>Acknowledges the currently selected clock divider value for the clock source selected by bit n. For example, GPUCLK_DIV2 acknowledges the divider value for the clock selected when CLKSELECT is 0x02.</p> <p>Currently selected clock divider value for the clock source selected by register GPUCLK_CTRL.</p> <p>Clock divider value = CLKDIV_CUR + 1.</p>
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	<p>GPUCLK_DIVn register requests a new clock divider value for the clock source selected by bit n. For example, GPUCLK_DIV2 selects the divider value for the clock selected when CLKSELECT is 0x02.</p> <p>Clock divider value = CLKDIV + 1.</p>

4.8.5 ACLKGPU_CTRL Register

The ACLKGPU_CTRL Register characteristics are:

Purpose

Selects the divider ratio for ACLKGPU. The input clock is GPUCLK.

Usage constraints

This register is read-write and read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the ACLKGPU_CTRL Register bit assignments.

Table 166: ACLKGPU_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:12]	CLKDIV_CUR	RO	Acknowledges the currently active clock divider value. Clock divider value = CLKDIV_CUR + 1.
[11:8]	-	-	Reserved.
[7:4]	CLKDIV	RW	Requests new clock divider value. Clock divider value = CLKDIV + 1.
[3:0]	-	-	Reserved.

4.8.6 CLKFORCE_STATUS Register

The bit allocation is the same as the CLKFORCE_SET register. If a bit reads as 1 then the associated dynamic clock gating is disabled, otherwise it is enabled. The CLKFORCE_STATUS Register characteristics are:

Purpose

Clock force status register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the CLKFORCE_STATUS Register bit assignments.

Table 167: CLKFORCE_STATUS Register bit assignments

Bits	Name	Type	Function
[31:4]	-	-	Reserved.
[3]	ELACKFORCE	RO	Clock status for ELA. This field is only available if CAP register bit 1 is set to a 1. Otherwise it is Reserved.
[2]	ACLKGPUFORCE	RO	Clock status for ACLKGPU.
[1]	GPUCLKFORCE	RO	Clock status for GPUCLK. This field is only available if CAP register bit 0 is set to a 1. Otherwise it is Reserved.
[0]	-	-	Reserved.

4.8.7 CLKFORCE_SET Register

Writing 1 to a bit within the CLKFORCE_SET register disables any dynamic hardware clock gating, while writing 0 to a bit is ignored. The CLKFORCE_SET Register characteristics are:

Purpose

Clock force set register.

Usage constraints

This register is write-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the CLKFORCE_SET Register bit assignments.

Table 168: CLKFORCE_SET Register bit assignments

Bits	Name	Type	Function
[31:4]	-	-	Reserved.
[3]	ELACKFORCE	WO	Write 0b1 to enable clock force for ELA. This field is only available if CAP register bit 1 is set to a 1. Otherwise it is Reserved.
[2]	ACLKGPUFORCE	WO	Write 0b1 to enable clock force for ACLKGPU.
[1]	GPUCLKFORCE	WO	Write 0b1 to enable clock force for GPUCLK. This field is only available if CAP register bit 0 is set to a 1. Otherwise it is Reserved.
[0]	-	-	Reserved.

4.8.8 CLKFORCE_CLR Register

The bit allocation is the same as the CLKFORCE_SET register. Writing 1 to a bit within the CLKFORCE_CLR register enables the dynamic hardware clocking gating, while writing 0 to a bit is ignored. The CLKFORCE_CLR Register characteristics are:

Purpose

Clock force clear register.

Usage constraints

This register is write-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the CLKFORCE_CLR Register bit assignments.

Table 169: CLKFORCE_CLR Register bit assignments

Bits	Name	Type	Function
[31:4]	-	-	Reserved.
[3]	ELACKFORCE	WO	Write 0b1 to clear (disable) clock force for ELA. This field is only available if CAP register bit 1 is set to a 1. Otherwise it is Reserved.
[2]	ACLKGPUFORCE	WO	Write 0b1 to clear (disable) clock force for ACLKGPU.
[1]	GPUCLKFORCE	WO	Write 0b1 to clear (disable) clock force for GPUCLK. This field is only available if CAP register bit 0 is set to a 1. Otherwise it is Reserved.
[0]	-	-	Reserved.

4.8.9 CAP Register

The CAP Register characteristics are:

Purpose

Set CAP value based on the configuration.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the CAP Register bit assignments.

Table 170: CAP Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1]	ELA support	RO	<p>0b0 - ELA is not supported</p> <p>0b1 - ELA is supported</p> <p>All the fields in the GPU Power Control registers pertaining to ELA are RAZ/WI if this bit is set to 0.</p>
[0]	GPUCLK Gating	RO	<p>0b0 - GPUCLK gating is not supported</p> <p>0b1 - GPUCLK gating is supported.</p>

4.8.10 PIK_POWER_CONTROL_LOGIC Register

The PIK_POWER_CONTROL_LOGIC configuration register characteristics are:

Purpose

Power control logic configuration register. The value is dependent upon chosen configuration.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the PIK_POWER_CONTROL_LOGIC Register bit assignments.

Table 171: PIK_POWER_CONTROL_LOGIC Register bit assignments

Bits	Name	Type	Function
[31:16]	-	RO	POWER CONTROL LOGIC_ID. It is set to 0x41.

Bits	Name	Type	Function
[15:4]	-	-	Reserved
[3:0]	no_of_ppu	RO	Defines the number of PPU's in the POWER CONTROL LOGIC. This value is set to 0x1 to indicate one PPU.

4.8.11 PID4 Register

The PID4 register characteristics are:

Purpose

Peripheral ID 4 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the PID4 Register bit assignments.

Table 172: PID4 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ.
[7:4]	4KB_count	RO	The number of 4KB address blocks required to access the registers, expressed in powers of 2. These bits read back as 0x4. This means that the POWER CONTROL LOGIC occupies 64KB address block.
[3:0]	jep106_c_code	RO	The JEP106 continuation code value represents how many 0x7F continuation characters occur in the identity code of the manufacturer. These bits read back as 0x4.

4.8.12 PID0 Register

The PID0 register characteristics are:

Purpose

Peripheral ID 0 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the PID0 Register bit assignments.

Table 173: PID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ.
[7:0]	part_number_0	RO	These bits read back as 0xB8.

4.8.13 PID1 Register

The PID1 register characteristics are:

Purpose

Peripheral ID 1 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the PID1 Register bit assignments.

Table 174: PID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:4]	jep106_id_3_0	RO	JEP106 identity code [3:0]. See the <i>JEDEC Standard Manufacturer's Identification Code</i> .
[3:0]	part_number_1	RO	These bits read back as 0x0.

4.8.14 PID2 Register

The PID2 register characteristics are:

Purpose

Peripheral ID 2 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the PID2 Register bit assignments.

Table 175: PID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:4]	Revision	RO	Identifies the revision of the base POWER CONTROL LOGIC. For revision r0p0, this field is set to 0x0.
[3]	jedec_used	RO	This indicates that the POWER CONTROL LOGIC uses a <i>manufacturer's identity code</i> that was allocated by JEDEC according to JEP106. This bit always reads back as 0x1.
[2:0]	jep106_id_6_4	RO	JEP106 identity code [6:4]. See the <i>JEDEC Standard Manufacturer's Identification Code</i> .

4.8.15 PID3 Register

The PID3 register characteristics are:

Purpose

Peripheral ID 3 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the PID3 Register bit assignments.

Table 176: PID3 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ

Bits	Name	Type	Function
[7:4]	RevAnd	RO	The top-level RTL provides a 4-bit input, ECOREVNUM, that is normally tied LOW and provides a read value of 0x0. When silicon is available, and if metal fixes are necessary, the manufacturer can modify the tie-offs to indicate a revision of the silicon.
[3:0]	mod_number	RO	This is set to 0x0.

4.8.16 Component ID0 Register

The ID0 register characteristics are:

Purpose

Component ID 0 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the Component ID0 Register bit assignments.

Table 177: Component ID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:0]	comp_id_0	RO	These bits read back as 0x0D.

4.8.17 Component ID1 Register

The ID1 register characteristics are:

Purpose

Component ID 1 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the Component ID1 Register bit assignments.

Table 178: Component ID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:0]	comp_id_1	RO	These bits read back as 0xF0.

4.8.18 Component ID2 Register

The ID2 register characteristics are:

Purpose

Component ID 2 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the Component ID2 Register bit assignments.

Table 179: Component ID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:0]	comp_id_2	RO	These bits read back as 0x05.

4.8.19 Component ID3 Register

The ID3 register characteristics are:

Purpose

Component ID 3 register.

Usage constraints

This register is read-only.

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [GPU clock and power control logic registers summary](#).

The following table shows the Component ID3 Register bit assignments.

Table 180: Component ID3 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved, SBZ
[7:0]	comp_id_2	RO	These bits read back as 0xB1.

4.9 Generic Timer registers

Morello supports timer frames and synchronization for multichip mode.

4.9.1 Generic Timer registers summary

The following table shows the Generic Timer registers in offset order from the base memory address. Undefined registers are reserved. Software must not attempt to access these registers.

Table 181: Generic Timer registers summary

Offset	Name	Type	Reset	Width	Description
-	MST_GCNT_SYNC_CTRL	-	-	32	See MST_GCNT_SYNC_CTRL Register .
-	LVCHIP_GCNT_SYNC_CTRL	-	-	32	See SLVCHIP_GCNT_SYNC_CTRL Register .
-	SLVCHIP_GCNT_INT_STATUS	-	-	32	See SLVCHIP_GCNT_INT_STATUS Register .
0x0028	SLVCHIP_GCNT_RETRY_CNT	RW	0x0	32	See SLVCHIP_GCNT_RETRY_CNT Register .

4.9.2 MST_GCNT_SYNC_CTRL Register

The MST_GCNT_SYNC_CTRL Register characteristics are:

Purpose

-

Usage constraints

-

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Generic Timer registers summary](#).

The following table shows the MST_GCNT_SYNC_CTRL Register bit assignments.

Table 182: MST_GCNT_SYNC_CTRL Register bit assignments

Bits	Name	Type	Function
[31:7]	-	-	Reserved.
[6:2]	TURN_AR_TIME	-	Number of clocks to wait between back to back start of the transactions as noted in the diagram attached
[1]	EN_SYNC_IMM	-	Enables immediate synchronization process
[0]	EN	-	Enable Sync process

4.9.3 SLVCHIP_GCNT_SYNC_CTRL Register

The SLVCHIP_GCNT_SYNC_CT Register characteristics are:

Purpose

-

Usage constraints

-

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See Generic Timer registers summary.

The following table shows the SLVCHIP_GCNT_SYNC_CT Register bit assignments.

Table 183: SLVCHIP_GCNT_SYNC_CT Register bit assignments

Bits	Name	Type	Function
[31:7]	-	-	Reserved.
[6:2]	TURN_AR_TIME	-	Number of clocks to wait between back to back start of the transactions for retries.
[1]	EN_SYNC_IMM	-	Enable immediate synchronization process.
[0]	EN	-	Enable synchronization process.

4.9.4 SLVCHIP_GCNT_INT_STATUS Register

The SLVCHIP_GCNT_INT_STATUS Register characteristics are:

Purpose

-

Usage constraints

-

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Generic Timer registers summary](#).

The following table shows the SLVCHIP_GCNT_INT_STATUS Register bit assignments.

Table 184: SLVCHIP_GCNT_INT_STATUS Register bit assignments

Bits	Name	Type	Function
[31:4]	-	-	Reserved.
[3]	Time out Interrupt	-	Time out interrupt when Master does not respond to sync request.
[2]	Sync failed interrupt status	-	Synchronization failed when software request by setting EN_SYNC_IMM register field.
[1]	Sync passed interrupt status	-	Synchronization passed when software request by setting EN_SYNC_IMM register field
[0]	Sync failed after number of retries specified	-	Synchronization failed after n-number of retries.

4.9.5 SLVCHIP_GCNT_RETRY_CNT Register

The SLVCHIP_GCNT_RETRY_CNT Register characteristics are:

Purpose

-

Usage constraints

-

Configurations

Available in all Morello configurations.

Memory offset and full register reset value

See [Generic Timer registers summary](#).

The following table shows the SLVCHIP_GCNT_RETRY_CNT Register bit assignments.

Table 185: SLVCHIP_GCNT_RETRY_CNT Register bit assignments

Bits	Name	Type	Function
[31:5]	-	-	Reserved.

Bits	Name	Type	Function
[4:0]	RETRY_COUNT	-	Retries before raising the interrupt and go into stall mode.

Appendix A Rainier clusters

This appendix is a short overview of the Rainier cluster and describes the CPU ID, to be used in conjunction with the *Arm® Architecture Reference Manual Supplement Morello for A-profile Architecture*.

A.1 About Rainier

The Rainier cluster is a high-performance and low-power Arm prototype dual-core element that implements the Armv8-A architecture.

The Rainier cluster supports:

- The Armv8.2-A extension.
- The RAS extension.
- The Statistical Profiling extension.
- ARMv8.3-RCpc, Weaker release consistency: three Load-Acquire RCpc Register (LDAPR) instructions are introduced by the Armv8.3-A extension.
- The Load acquire (LDAPR) instructions introduced in the Armv8.3-A extension.
- ARMv8.0-SSBS, Speculative Store Bypass Safe bit: The PSTATE.SSBS bit is added to allow software to indicate whether hardware is permitted to load or store speculatively in a manner that could give rise to a cache timing side channel, which in turn could be used to derive an address from values loaded to a register from memory.
- ARMv8.2-DotProd, SIMD Dot Product: The SIMD dot product instructions are added to the A64 and A32/T32 instruction sets.



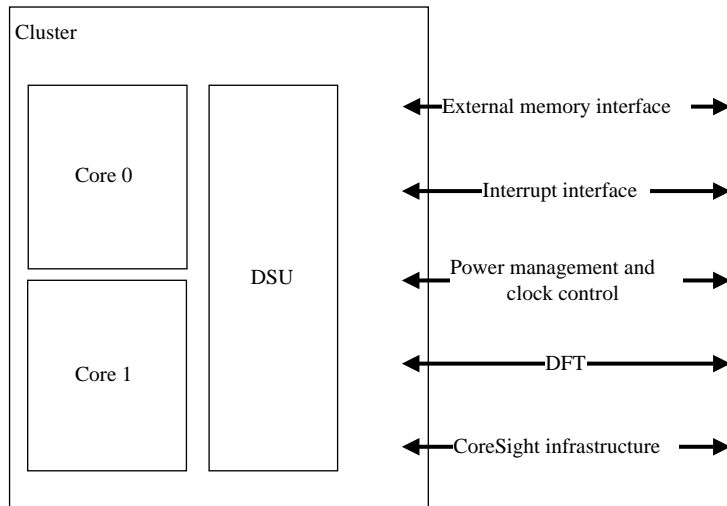
Note

The Morello architecture is supported in AArch64 state only. Morello introduces a new data type to Arm®v8-A architecture profile, Capability, an unforgeable token of authority that provides a foundation for fine-grained memory protection and strong compartmentalization. The architecture extends the Arm®v8 AArch64 state with the principles proposed in version 8 of the Capability Hardware Enhanced RISC Instructions: CHERI Instruction-Set Architecture, to provide hardware support for fine-grained protection, and building blocks for secure, scalable compartmentalization.

For a full description of the Armv8-A architecture capability profile, read the *Arm® Architecture Reference Manual Supplement Morello for A-profile Architecture*.

The following figure shows the Rainier cluster.

Figure 10: Rainier cluster



Rainier has a Level 1 (L1) memory system and a private, integrated Level 2 (L2) cache. It also includes a superscalar, variable-length, out-of-order pipeline.

Rainier is implemented inside the DynamIQ Shared Unit (DSU) cluster.

A.2 Rainier features and components

The Rainier clusters in the Morello SoC contain the following features and components.

Major components of the Rainier clusters in the Morello SoC

The Morello SoC contains two dual-core Rainier clusters. Each cluster has:

- 64KB private L1 instruction cache for each core.
- 64KB private L1 data cache for each core.
- 1MB private L2 unified cache for each core.
- 1MB shared L3 unified cache in the DynamIQ Shared Unit (DSU) Flash Cache Module (FCM).
- Digital Storage Oscilloscope (DSO) for voltage sensing and logic monitoring, with current stimulus generated by a separate Noise Generator (NG).

Core features

The major features of the Rainier cores are:

- 48-bit Physical Address (PA).

- Memory Management Unit (MMU).
- Cryptographic Extension.
- Superscalar, variable-length, out-of-order pipeline.
- Support for Arm TrustZone® technology.
- Reliability, Availability, and Serviceability (RAS) Extension.
- Generic Interrupt Controller (GICv4) CPU interface to connect to an external distributor.
- Generic Timers interface supporting 64-bit count input from an external system counter.
- Integrated execution unit that implements the Advanced SIMD and floating-point architecture support.
- AArch64 Execution state at all Exception levels (EL0 to EL3).

Cache features

The Rainier cache features are:

- Separate L1 data and instruction caches.
- Private, unified data and instruction L2 cache.
- L1 and L2 memory protection in the form of Error Correcting Code (ECC) or parity on RAM instances which affect functionality.
- Configurable instruction cache hardware coherency.

Debug features

The Rainier debug features are:

- Armv8.2 debug logic.
- Performance Monitoring Unit (PMU).
- Statistical Profiling Extension (SPE).
- CoreSight Embedded Logic Analyzer (ELA).
- Embedded Trace Macrocell (ETM) that supports instruction trace only.

Rainier core components

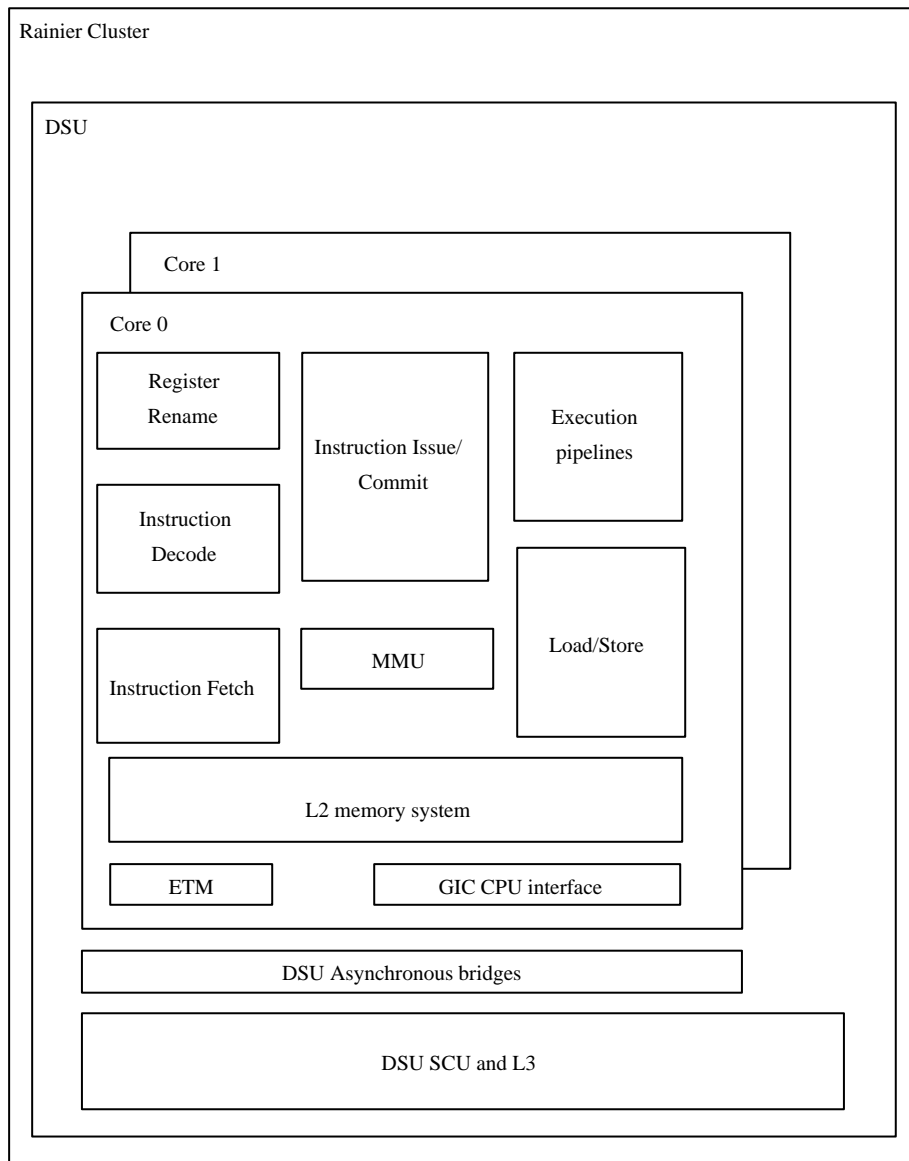
The main components of the Rainier core are:

- Instruction fetch
- Instruction decode
- Register rename
- Instruction issue
- Execution pipelines

- L1 data memory system
- L2 memory system

The following figure is an overview of the Rainier cores.

Figure 11: Rainier core overview



Instruction fetch

The instruction fetch unit fetches instructions from the L1 instruction cache and delivers the instruction stream to the instruction decode unit.

The instruction fetch unit includes:

- 64KB, 4-way, set associative L1 instruction cache with 64-byte cache lines and parity protection.
- Fully associative L1 instruction TLB with 64KB page sizes.
- Dynamic branch predictor.
- Configurable support for instruction cache hardware coherency.

Instruction decode

The instruction decode unit supports the A64 instruction set. It also supports Advanced SIMD and floating-point instructions.

Register rename

The register rename unit performs register renaming to facilitate out-of-order execution and dispatches decoded instructions to various issue queues.

Instruction issue

The instruction issue unit controls when the decoded instructions are dispatched to the execution pipelines. It includes issue queues for storing instruction pending dispatch to execution pipelines.

Execution pipeline

The execution pipeline includes:

- Integer execute unit that performs arithmetic and logical data processing operations.
- Vector execute unit that performs Advanced SIMD and floating-point operations. It can execute the cryptographic instructions.

L1 data memory system

The L1 data memory system executes load and store instructions and encompasses the L1 data side memory system. It also services memory coherency requests.

The load/store unit includes:

- 64KB, 4-way, set associative L1 data cache with 64-byte cache lines and ECC protection per 32 bits.

- Fully associative L1 data TLB with 64KB page sizes.

L2 memory system

The L2 memory system services L1 instruction and data cache misses in the Rainier core.

The L2 memory system includes:

- 8-way set associative L2 cache with data ECC protection per 64 bits. The L2 cache is 1024KB.
- Interface with the DynamIQ Shared Unit (DSU) configured for asynchronous operation.

A.3 Main ID Register, MIDR_EL1

The MIDR_EL1 provides identification information for the Rainier core, including an implementer code for the device and a device ID number.



For general Rainier programming information, see *Arm® Architecture Reference Manual Supplement Morello for A-profile Architecture*.

Bit field descriptions

MIDR_EL1 is a 32-bit register. This register is read-only. The full register reset value is 0x3F0F_4120.

Figure 12: Rainier MIDR_EL1 bit assignments

31	24	23	20	19	16	15	8	7	4	3	0
Implementer				Variant		Architecture		PartNum		HW	Revision

Implementer, [31:24]

Indicates the implementer code. This code value is 0x3F - University/research.

Variant, [23:20]

Indicates the variant number of the core. This number is the major revision number x in the rx part of the rpxy description of the product revision status. This value is 0x0 - revision 0.

Architecture, [19:16]

Indicates the architecture code. This value is 0x0F - CPUID scheme.

PartNum, [15:8]

Indicates the primary part number. This value is 0x41 - Rainier core (Morello).

HW, [7:4]

Indicates hardware number. This value is 0x2 - Morello SoC.

Revision, [3:0]

Indicates the minor revision number of the core. This is the minor revision number y in the py part of the rpxy description of the product revision status. This value is 0x0 - part 0.

Configuration

The MIDR_EL1 is architecturally mapped. Bit fields and details are defined in the *Arm® Architecture Reference Manual Supplement Morello for A-profile Architecture*.

Appendix B CMN-Skeena

This appendix is a short overview of the CMN-Skeena coherent interconnect, within Morello.

B.1 About CMN-Skeena coherent mesh network

CMN-Skeena is a prototype coherent interconnect designed to enable the transportation of tags from Rainier cores to DMC-Bing.

CMN-Skeena, the primary interconnect in Morello, is based on the Arm® CoreLink™ CMN-600 Coherent Mesh Network product, itself a configurable coherent interconnect designed to meet the Power, Performance, and Area (PPA) requirements for coherent mesh network systems that are used in high-end networking and enterprise compute applications. The Morello platform implements the CHERI Capability extension to the Arm architecture in the form of tagged bits. The modifications to CMN-600 that have resulted in CMN-Skeena include:

- An additional 129th bit to data path.
- An additional transport bit in existing packets, known as a “Poison” bit.
- An updated SLC: the poison status is stored as special encoding of ECC in RAMs.
- Poison generation/handling is disabled to ensure propagation of bit.

For more information on CMN-600, see the *Arm® CoreLink™ CMN-600 Coherent Mesh Network Technical Reference Manual*. For more information on the capability architecture, see the *Arm® Architecture Reference Manual Supplement Morello for A-profile Architecture*.

Compliance

CMN-Skeena is based on the AMBA 5 CHI Issue E architecture specification, and implements the following capabilities:

- Fully compliant with CHI interconnect architecture.
- Non-blocking coherence protocol.
- Packet-based communication.
- The following four types of channels:
 - Request (REQ).
 - Response (RSP).
 - Snoop (SNP).
 - Data (DAT).
- Credited end-to-end protocol-layer flow-control with a retry-once mechanism for flexible bandwidth and resource allocation.

- Integrated end-to-end Quality-of-Service (QoS) capabilities.
- See the *AMBA® 5 CHI Architecture Specification* for more information.

CMN-Skeena features

CMN-Skeena provides the following features:

- 5 x 2 mesh network topology.
- Two Fully coherent Requesting Node (RN-F) interfaces to CHI.E-based Rainier compute clusters.
- Two RN-F interfaces to CHI.E-based DMC-Bing memory controllers.
- 4MB system cache size.
- 8MB Snoop Filter (SF)
- I/O Home Node (HN-I) for a direct connection to CCIX AXI-slave interface to enable low latency pathways.
- Data channel: a pair of 256-bit data channels, one for each direction.
- DVM message transport between masters.
- QoS regulation for shaping traffic profiles.
- A Performance Monitoring Unit (PMU) to count performance-related events.
- RAS features including transport parity, optional data path parity, and SECDED ECC.

CMN-Skeena and Morello SoC connections

CMN-Skeena contains the following protocol nodes and devices:

RN-F (Fully coherent Requesting Node)

A fully coherent master device that supports CHI.E RN-F

RN-D (I/O coherent Requesting Node with DVM support) bridge

An I/O coherent master device that supports accepting DVM messages on the snoop channel.

HN-F (Fully coherent Home Node)

A device that acts as a home node for a coherent region of memory, accepting coherent requests from RN-Fs and RN-Is, and generating snoops to all applicable RN-Fs in the system as required to support the coherency protocol.

HN-I (I/O Home Node)

A device that acts as a home-node for the slave I/O subsystem, responsible for ensuring proper ordering of requests targeting the slave I/O subsystem. HN-I supports AMBA AXI or ACE-Lite.

HN-D (HN-I + DVM Node)

A device that includes HN-I, DVM Node (DN), Configuration Node (CFG), Global Configuration Slave, and the Power/Clock Control Block (PCCB).

SN-F (CHI Slave Node)

A device which solely is a recipient of CHI commands, limited to fulfilling simple read, write, and CMO requests targeting normal memory.

SBSX bridge

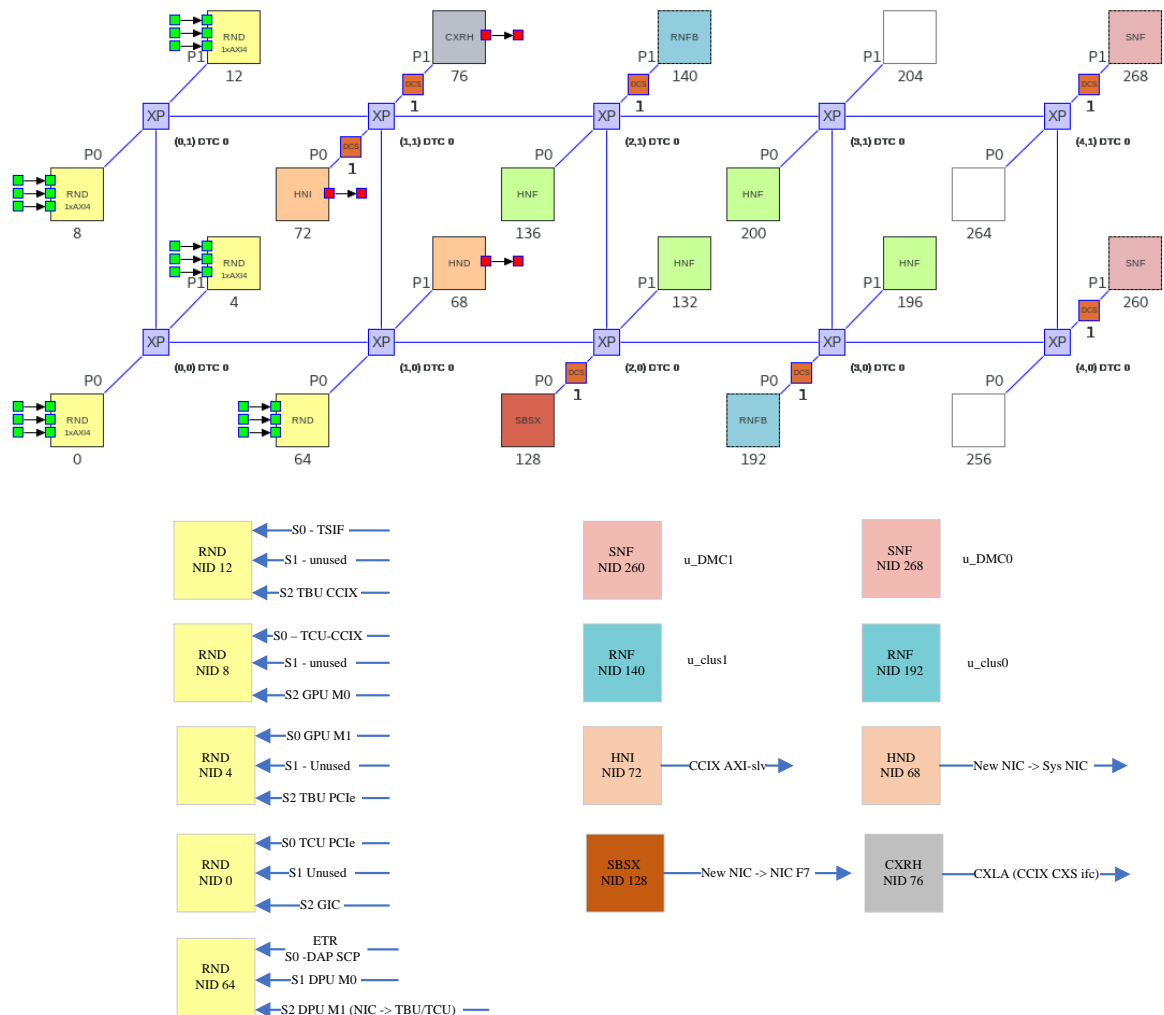
A CHI bridge device that converts simple CHI read, write, and CMO commands to an ACE-Lite slave memory device.

CXG bridge

A CXG device bridges between CHI and CXS (CCIX port) and contains: CCIX Request Agent (CXRA) proxy and CCIX Home Agent (CXHA) proxy functionality; CXS Link Agent (CXLA) functionality which is external to the CMN-600 hierarchy.

The following figure shows the CMN-Skeena mesh diagram, listing external SoC connections.

Figure 13: CMN-Skeena mesh and SoC connections



Appendix C DMC-Bing

This appendix is a short overview of DMC-Bing dynamic memory controller. It includes new DMC-Bing system registers and a brief description of the Client mode and Server mode.

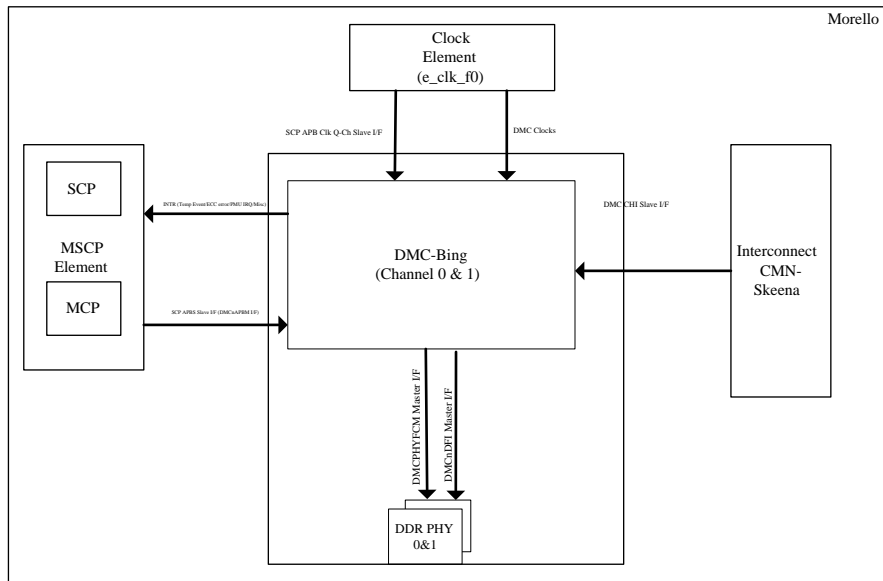
C.1 About DMC-Bing dynamic memory controller

DMC-Bing is a prototype CHERI-extended dynamic memory controller designed to support two different implementations of physical memory tagging. For more information on the capability architecture, see the *Arm® Architecture Reference Manual Supplement Morello for A-profile Architecture*.

DMC-Bing is based on the Arm® CoreLink™ DMC-620 Dynamic Memory Controller product, a high-performance, area-optimized memory controller that is compatible with the AMBA 5 CHI protocol. DMC-620 enables data transfer between the SoC and the SDRAM devices external to the chip. It connects to the on-chip system through a single CHI interface, and to a processor through the programmers APB3 interface to program the DMC-620. It connects to the SDRAM devices through its memory interface block and the DDR PHY Interface (DFI). See the *Arm® CoreLink™ DMC-620 Dynamic Memory Controller Technical Reference Manual*, for more information.

Morello has two DMC-Bing controllers, both are wrapped in a separate hierarchy, `soc_dds_phy_dmc_wrap`, with DDR PHY and other integration logic, and connected to the two DDR SoC interfaces. The following figure shows the DMC-Bing interfaces in Morello.

Figure 14: DMC-Bing connectivity



Compliance

DMC-Bing is compatible with the following protocol specifications and standards:

- AMBA 5 CHI-B protocol.
- AMBA 3 APB protocol.
- JEDEC DDR4 JESD79-4 standard.
- JEDEC DDR3 JESD79-3 standard.
- JEDEC DDR3L JESD79-3-1 standard.
- JEDEC JESD82-29 standard.
- JEDEC LRDIMM DDR4 Data Buffer Specification.
- DDR4 RCD02 Specification.
- DDR4 SDRAM Registered DIMM Design Specification.
- DDR4 SDRAM Load Reduced DIMM Design Specification.
- JEDEC JESD245 NVDIMM-N Byte Addressable Energy Backed Interface Specification.
- DFI 3.1.
- DFI 4.0.

Features

DMC-Bing has the following features:

- Two implementations of physical CHERI-based memory tagging:
 - Server mode: ECC bits hold tags.
 - Client mode: Tag controller and tag cache hold tags.
- 128-bit DMC queue depth.
- 256-bit DMC system data width.
- Profiling signals that enable performance profiling to be performed in the system.
- Buffering to optimize read and write turnaround, and to maximize bandwidth.
- A System Interface (SI) that provides:
 - A CHI interface to connect to a CoreLink Coherent Mesh Network (CMN).
 - An AMBA5 CHI interface supporting the CHI-B architecture.
 - An APB interface for configuration and initialization.
 - 256-bit CHI interface
- A Memory Interface (MI) that provides:
 - A DFI 3.1 and 4.0 interface to a PHY that supports DDR4.
 - Support for 1:2 DFI frequency ratio mode.
- Low-power operation through programmable SDRAM power modes.
- ARMv8.2 compatible Reliability, Availability, Serviceability (RAS):
 - Symbol-based ECC, to correct memory chip and data-lane failures.
 - Supports ARMv8.2 end-to-end RAS protection and deferment.
 - Hardware Read-Modify-Write (RMW) for systems supporting sparse writes.
 - Command-Address (CA) parity checks for DDR4 link faults.
 - CRC write-data protection for DDR4 devices.
- A programmable mechanism for automated SDRAM scrubbing.
- Error handling and automated recovery.
- Power Control Logic (PCL) that generates powerdown requests to the SDRAM, and manages power enables for the PHY logic.
- 3DS support for 8H, 4H, and 2H devices.
- DDR4 Registered Dual In-line Memory Module (RDIMM) and Load-Reduced Dual In-line Memory Module (LRDIMM) support.
- Flexible Dual In-line Memory Module (DIMM) topology support:
 - Signal multiplexing that allows a single board layout to support different RDIMM device types (3DS or planer), and a different number of devices.
 - Support for RDIMM Encoded or Direct CS.

- Core to DMC Prefetch Hint direct path allowing the core to directly initiate a DMC prefetch.

Morello Capabilities and DMC-Bing

Every 128 bits of data has a tag bit:

- Tag = 1, ptr is a valid capability.
- Tag = 0, ptr is not a valid capability.

Capability tags are stored with data in caches and in a dedicated region of DRAM. The Tag Cache, which resides in the memory element, converts from tag-aware parts of the system, such as CMN-Skeena, to tag-unaware parts of the system, such as DRAM. Only the Rainier cores can set a tag bit, while other IP can clear a tag bit, such as when an error condition is detected.

In Morello, a tag bit, the 129th bit, is delivered to the memory system over the poison bits. Poison bits are used exclusively for tag bits and do not carry any type of error information:

- One poison bit per 64 bits of data.
- Two poison bits per 128 bits of data.
- The two poison bits must always be the same value.
- Assertions in place to detect 2'b01 and 2'b10 cases.
- Bing logically ANDs the 2 bits to force tag bit = 0.

Server mode and Client mode

DMC-Bing operates in two different modes: Client mode and Server mode. Tags are always enabled in both modes.

In Server mode, a capability tag bit is carried in the DRAM ECC field along with the ECC bits. Server mode involves changing the way ECC is calculated and consumed within DMC-Bing. ECC is calculated across 128 bits. The syndrome is modified for SECDED across 128-bits, and the recovered bit is used to store the tag.

Client mode involves adding a tag cache between the system interface of DMC-Bing and the rest of the DMC.

First, the tag is split from the transaction:

1. A new transaction to memory is created to transfer this tag to an appropriate location in memory.
2. A transaction tracker is allocated to track the lifetime of this tag transaction.
3. Read Responses for the tag transaction are merged with the read response for the parent request.
4. Write responses to the tag transaction are silently discarded, since the interface is strongly ordered.

Second, the tag transaction is passed through an invisible write-back cache:

1. Cache line is 64B, to match the DDR4 x64 interface that DMC-Bing supports.
2. Out of reset, the cache is optionally initialised to 0.
3. Writes that set capabilities are always installed in the cache. Writes that clear capability are evicted from the cache.
4. Retrieved tags (that are set) are allocated into the cache.
5. Replacement policy is to use LRU.

A further optimisation seeks to compress the area needed on chip to efficiently cache information that tags in a table format:

1. The table seeks to eliminate the metadata access where possible by providing a filter for non-capability locations. Where it can conclude that capability is absent, the metadata access can be pre-empted.
2. The table works as a coarse map of the capability information. In its simplest form, a one-bit entry in the table is an OR-reduction of the 512-bits of a line of metadata, which indicates the possibility of capability for their respective real data locations. Out of reset, it is assumed no location has capability and so the table is “empty”.
3. In a multi-level table, the local physical copy of the table can be sparsely populated such that only the root table covers the whole metadata region. Any leaf tables can be kicked out to cache and/or DRAM in spare regions of memory. In this way, adaptable table schemes can be devised.

All capabilities are in the tag cache. Anything that is not in the cache does not have capabilities. The tag cache operates in the following way:

1. When the cache is full, it needs to install metadata in the directory. The directory can be exclusive of cache but may speed up cache lookups if it is inclusive until full.
2. To prevent unnecessary off-chip metadata retrieval, the cache must refine directory entries as finely as possible.

The tags are stored in a special carve-out region of memory:

1. Top 128th of addressable DRAM is reserved for Morello:
 - a. Software performs this reservation, the effect of which is to reduce the amount of DRAM available to the memory allocator.
 - b. The hardware does not restrict direct access to this address space, the Morello debugger has direct access to this space.
 - c. The tag cache must be programmed with the base physical address of the region.
 - d. The region must be a contiguous range of physical address.
2. Each Data location has a corresponding tag location:
 - a. 4-bits per 64B data cache line.
 - b. 64B tag cache line corresponds to 128 data cache lines, or 8KB of memory.

3. The tag cache is behind DRAM address translation, so it:
 - a. Is in a contiguous address space local to that memory channel.
 - b. Needs to divide by data to tag ratio and add the reserved region base address relative to the size of memory addressed by this channel.

C.2 Bing system registers

In addition to the existing DMC-600 system registers, DMC-Bing has six new performance counters.

Table 186: Bing system registers

Bits	Name	Type	Reset	Width	Description
0xD00	capability_ctl	RW	0	1	0 +: 1 capability_mode 0 = server mode 1 = client mode
0xD04	tag_cache_ctl	WO	0	1	0 +: 1 invalidate_all
0xD08	tag_cache_cfg	RW	3'b111	3	0 +: 1 l1_tag_cache_en 1 +: 1 c1_tag_cache_en 2 +: 1 c2_tag_cache_en
0xD0C	memory_access_ctl	RW	0_0f0 f	12	0 +: 4 read_qos 8 +: 4 write_qos 16 +: 1 memory_access checking disable
0xD10	memory_address_ctl	RW	0	32	0 +: 32 carve_out_base_address _31_0
0xD14	memory_address_ctl2	RW	0	32	0 +: 32 carve_out_base_address _64_32
0xD18	bing_special_ctrl_reg	RW	0	32	0 +: 32 bing_special_ctrl

Client mode and feature_config register

The feature_config register controls the DMC features. In Client mode configuration, you must set bit 8 *si_clk_gate_disable* of the feature_config register to 0b1.

The feature_config register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Offset

0x130

Type

Read-write. Can be read from ALL states. Can be written when in CONFIG or LOW-POWER states.

Reset

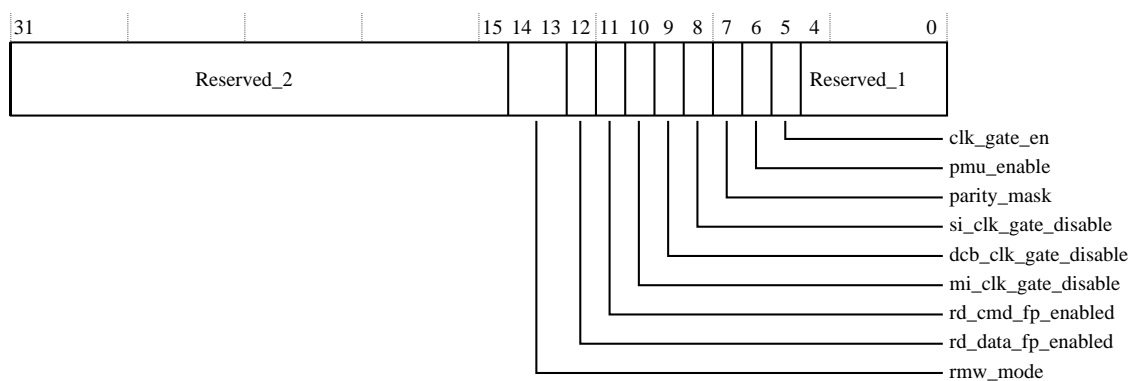
0x000018E0

Width

32

The following figure shows the bit assignments.

Figure 15: feature_config bit assignments



For Client mode configuration, bit 8 *si_clk_gate_disable* of the feature_config register offset 0x130 must be set to 0b1. If not set, the behavior in Client mode will be unpredictable.

Appendix D Revisions

This appendix describes the technical changes between released issues of this book.

Table 187: Issue 0000-01

Change	Location	Affects
First release.	-	-

Table 188: Differences between issue 0000-01 and 0000-02

Change	Location	Affects
Added new topic, Client mode and feature_config register, to the DMC-Bing appendix. It describes the bit assignments and the requirement to set bit 8, si_clk_gate_disable, when in Client mode.	DMC-Bing	All revisions.